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A Publication
for the Radio-Amateur

Especially Covering VHF,
UHF and Microwaves

VHF communications

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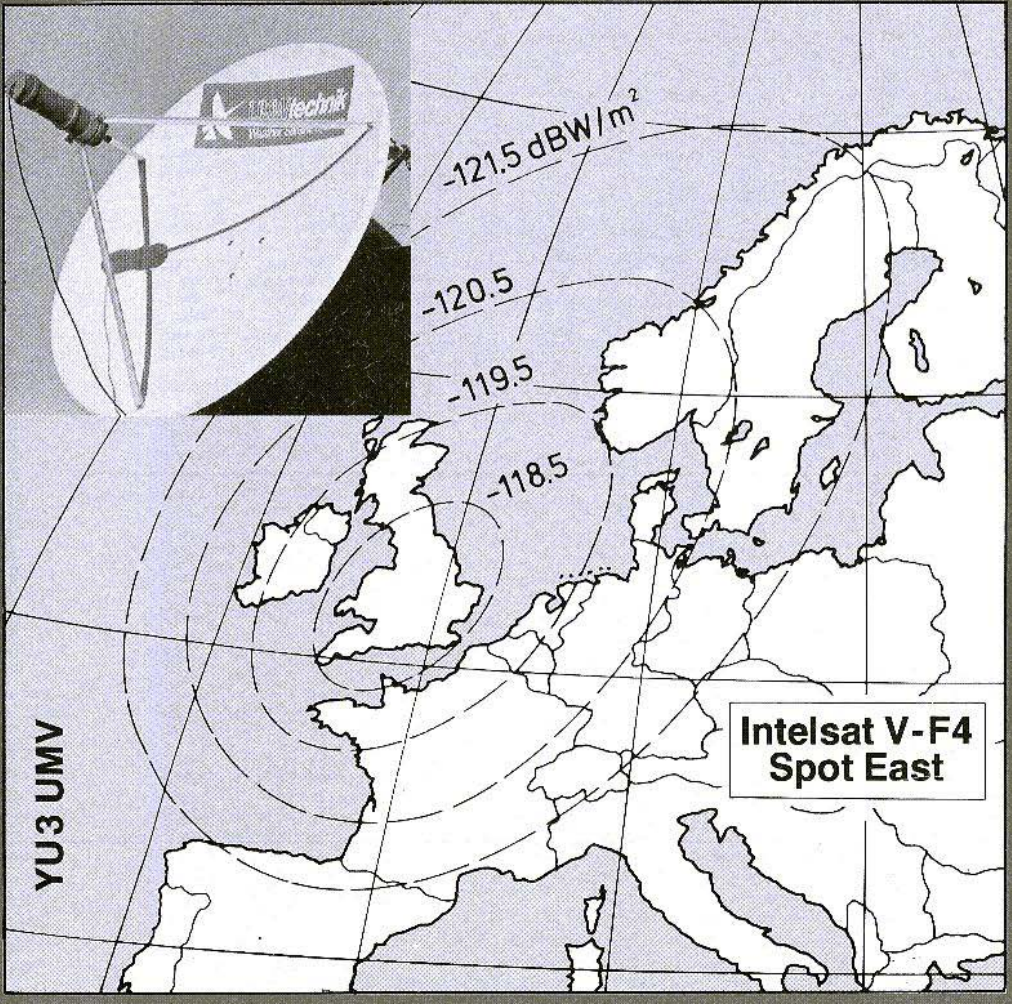

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Contents

The staff of VHF COMMUNICATIONS wishes all readers a **Happy and Prosperous New Year**. As a foretaste for the 1987 editions, I will list here some articles which are in preparation, e.g.:

M. Vidmar: TV Satellite Receive System. Part 2: Indoor Unit
J.Kestler: PLL Oscillators with Delay Lines. Part 5: Digital Frequency Tuning.
W. Borschel: Dimensioning Stacked Yagi Antennas Using the Superposition Technique.
D. Dobričić: A 250 W PA for 23 cm
J. Jirmann: A Home-Made Spectrum Analyzer (0 - 500 MHz)
R. Oppelt: The Generation and Demodulation of SSB Signals Using the Phasing Method

The Editor

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Matjaž Vidmar, YT 3 MV (ex YU 3 UMV)

TV Satellite Receive System
Part 1: Low-Noise 11 GHz Down-Converter

The professional engineer, Matjaž Vidmar, who has become a world-wide known author following his weather satellite picture memory (VHF COMMUNICATIONS 4 / 1982, 1 and 2 / 1983), describes in this series an installation for the reception of communication satellites. The complete installation is intended as a constructional project for the experienced radio amateur.

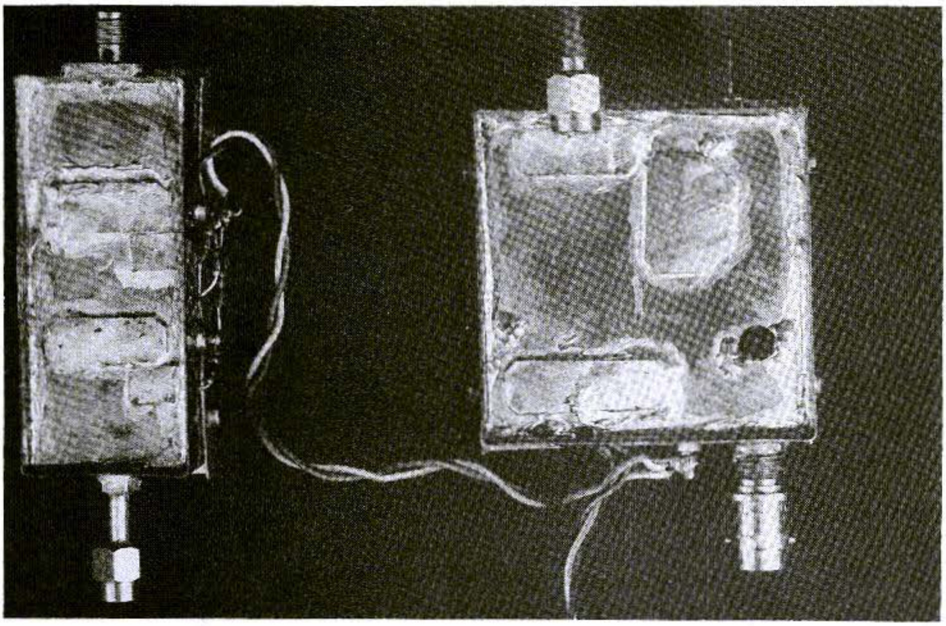
The extensive nature of this publication recessitates its division into several articles, forming a series, which will take the constructional process right through to the vision and sound outputs. The article will be complete and with no need for "supplementary" modules.

Although the construction and alignment will be relatively detailed, it is recommended that the author's article "Microstrip Transverters for 23 and 13 cm" in VHF COMMUNICATIONS 2 and 3 / 1986 should be studied. Part 2, in particular, contains a wealth of "know how" for constructional practice at microwave frequencies.

1. INTRODUCTION

The frequency band between 10.95 and 12.75 GHz is allocated as a downlink band for many different satellite services. The subband from 10.95 to 11.7 GHz and in particular the two segments from 10.95 to 11.2 GHz and from 11.45 to 11.7 GHz are allocated as the downlink bands for international satellite communications including both telephone circuits and international television distribution. The subband between 11.7 and 12.5 GHz will probably be used by the powerful direct broadcast television satellites. Finally the segment from 12.5 to 12.75 GHz is again being used for national and international satellite communications including telephone circuits, data transmissions and television distribution.

Communications satellites are usually launched into geostationary orbits about 36 000 km above the earth's equator. The distance from user stations, accessing the satellite, is therefore in the 40 000 km range. Present satellites only carry rather weak transmitters, the output power per channel ranges from 5 to 40 W for communications satellites and will reach 250 W for high-power direct broadcast satellites. Of course, weak satellite signals require large receiving antennas. Fortunately, satellites transmitting in the Ku-band usually use high-gain spot beam antennas of just a few degrees total beamwidth to cover populated areas on the globe, like Western Europe, where most user stations are located. Television transmissions, coming from these satellites, can be received with moderately sized antennas, usually parabolic dishes of less than 3 m diameter, and are being used to feed large cable TV networks.



Photograph A: Bottom view of the pre-amplifier and converter

In amateur conditions, an excellent noise-free picture can be obtained with parabolic dishes of less than 2 m diameter even from low-power communications satellites carrying 10 or 20 W transmitters like the INTELSAT V and VA, ECS EUTELSAT and TELECOM 1 satellite series.

A satellite TV receiving station includes a parabolic dish antenna, a suitable receiver and an ordinary TV set or monitor. The first receive down-converter is equipped with a low-noise preamplifier and is usually installed directly behind the antenna feed to avoid lossy and expensive microwave transmission lines. The remaining components of a satellite TV receiver are usually installed indoors and include a second tunable converter for channel selection, a second IF amplifier and FM video demodulator, a sound IF and demodulator, an AM modulator to generate a standard TV signal and a power supply for the complete receiver.

2. BLOCK DIAGRAM OF THE DOWN - CONVERTER

The block diagram of the Ku-band low-noise down-converter is shown in **fig. 1** together with the other outdoor component, a parabolic reflector antenna with a suitable feed for operation in the Ku - band.

Most available Ku-band satellite TV transmissions require a parabolic dish of 1.2 to 1.8 m diameter for noise-free reception in Western Europe depending on the particular satellite transmitter output power, antenna pattern and transponder mode of operation (half / full). Most available dishes, either new or surplus, have a focal to diameter (f / D) ratio of 0.35 to 0.40. A suitable feed for this f / D ratio is a circular waveguide horn with a corrugated flange for improved illumination efficiency. Since in the practical construction and alignment the feedhorn is a functional part of the down-converter, it will also be described in this article.

The low-noise down-converter includes three modules:

a. A low-noise amplifier for 10.95 to 11.7 GHz
b. A block down-converter 10.95 to 11.7 GHz / 0.85 to 1.6 GHz
c. An IF amplifier for 0.85 to 1.6 GHz.

The two-stage low-noise amplifier uses two 0.5 μm gate length gallium arsenide FETs (CFY 18 - 23, Siemens) mounted on a 0.5 mm thick glassfiber-teflon laminate. The block down-converter module includes a fixed tuned FET oscillator at 10.1 GHz, a single-ended active mixer stage using a 1 μm gate length gallium arsenide FET (CFY 19) and an IF preamplifier stage. The block down-converter module is also built on a 0.5 mm thick glassfiber-teflon laminate.

The IF amplifier module includes three amplifier stages using silicon bipolar microwave transistors and a + 5 VDC supply regulator for the other two modules equipped with GaAsFETs.

All the Ku-band connections are made with short lengths of RG-141, 3.6 mm diameter semirigid cable and SMA connectors. BNC connectors are used in the IF frequency range.

The low-noise down-converter requires a supply voltage of + 12 VDC. A practical solution is to feed the supply voltage through the same coaxial cable feeding the IF signal to the indoor unit. The same solution is being used with almost all commercially available low-noise down-converters.

The low-noise down-converter was originally designed for the 10.95 to 11.7 GHz satellite band since most satellites transmit in this frequency range. The circuit can also be modified to operate in the 12.5 to 12.75 GHz satellite band and the necessary modifications will be described later in this article. All the values given in the circuit diagrams and the dimensions given in the drawings, however, apply to the standard 10.95 to 11.7 GHz version!

3. DESCRIPTION OF THE OUTDOOR UNITS

3.1. Corrugated Horn Feed

The corrugated horn feed, shown in **fig. 2** , is made of a short length of circular waveguide, whose open end acts as the horn aperture, a waveguide to coax transition and an adjustable corrugated flange.

To achieve a good illumination efficiency, the feed horn should illuminate the parabolic dish surface as uniformly as possible with little spillover. Of course the beamwidth of the feed should be matched to the focal aperture angle of the parabolic dish used. This angle is in turn determined by the dish focal to diameter ratio. The beamwidth of a circular waveguide horn feed is mainly determined by the internal diameter of the waveguide. The dimensions, shown in **fig. 2**, are suitable for parabolic reflectors having a f / D ratio between 0.35 and 0.40.

The corrugated flange improves the illumination uniformity and decreases the sidelobes of the horn feed. The illumination efficiency may exceed 75 % and this brings an improvement of between 0.5 and 1 dB in the overall antenna gain. In the case of space communications, a decrease of the effective antenna temperature, due to the reduced spillover, should also be noted. A very simple explanation of the principle of operation of a corrugated surface (flange) is as follows: The corrugated surface enforces two boundary conditions; The tangential electric field should be zero due to the conductive rims and the tangential magnetic field should also be zero due to the $\lambda / 4$ deep corrugations between the rims. The combined effect of both boundary conditions is that the field intensity must fall to zero on the flange surface. This produces a rotationally symmetrical flat topped beam with very low sidelobes which is ideal for the illumination of parabolic reflectors.

A corrugated surface is also called a scalar surface in the literature since it behaves exactly in the

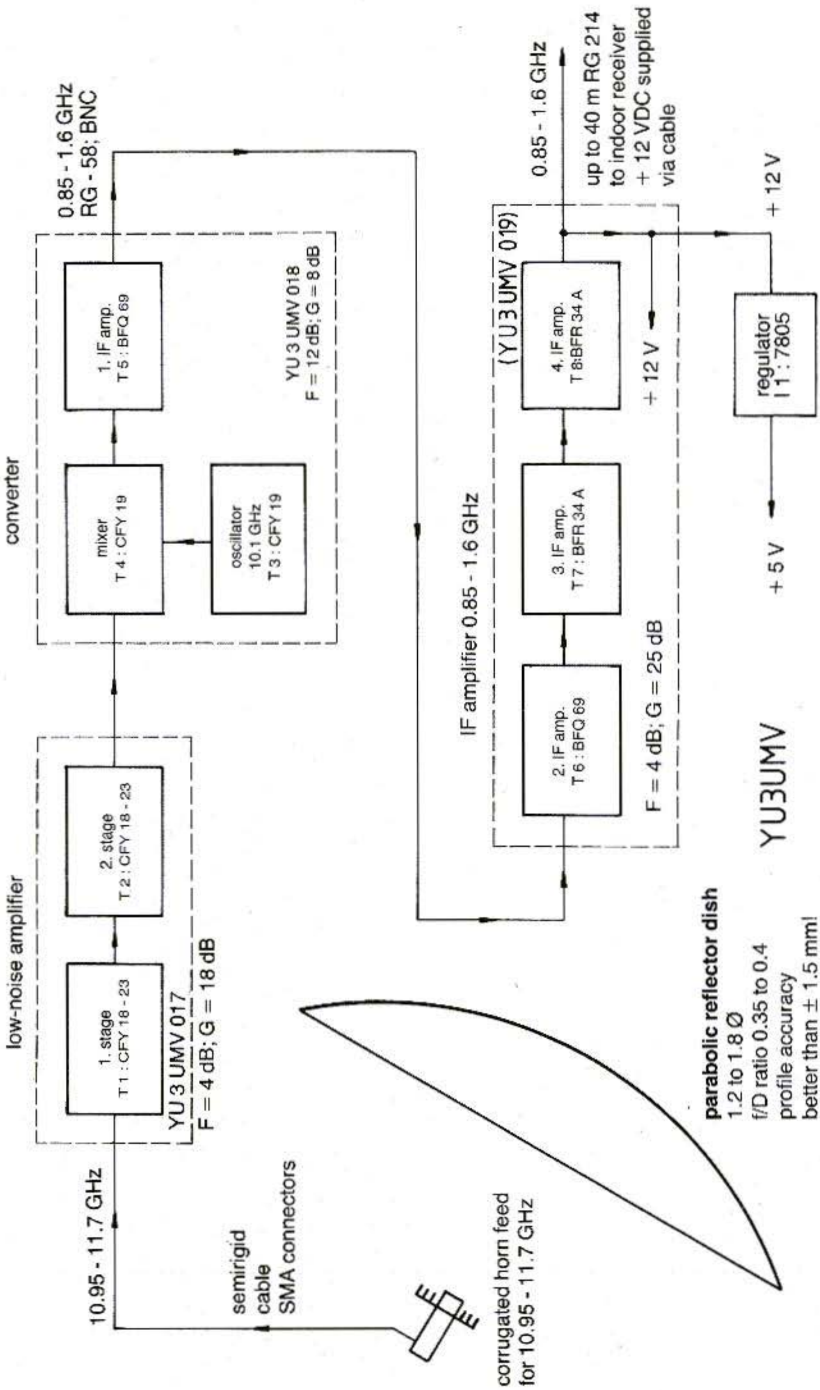


Fig. 1: Blockdiagram of the TV Satellite Receive System's outdoor units

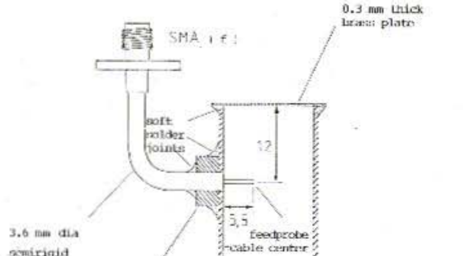


Fig. 2: Corrugated horn feed for 10.95 to 11.7 GHz

same way for both magnetic and electric fields. Correspondingly corrugated horns are also called scalar horns.

The position of the corrugated flange along the waveguide should be adjusted for best results. Usually the distance between the open end of the waveguide and the surface of the corrugated flange ranges between zero and $\lambda / 4$.

A circular waveguide horn can receive and / or transmit arbitrarily polarized waves, including two independent orthogonally polarized waves at the same time. The actual polarization of the horn feed therefore only depends on the waveguide mode launcher used – the coax to waveguide transition. Since most low-power satellites use linear polarization, either in a single plane or in two orthogonal planes for frequency re-use purposes, a linearly polarized feed is required. A suitable mode launcher is a simple $\lambda / 4$ probe inserted in the waveguide wall about $\lambda g / 4$ from the waveguide's shorted end, where λg is the wavelength inside the waveguide. Of course, the mechanical support structure must allow a smooth and easy adjustment of the feed polarization plane.

High-power direct broadcast satellites will probably use circular polarization, both right-hand and left-hand, between 11.7 GHz and 12.5 GHz. Circular polarization can simply be obtained from a linearly polarized mode inside a circular waveguide by inserting a few tuning screws at 45° with respect to the polarization plane of the linearly polarized mode.

3.2. Low-Noise Amplifier

The main function of the low-noise RF amplifier (see **fig. 3**) is to improve the overall down-converter noise figure. Besides having a low-noise figure, it should also have sufficient gain to prevent the overall noise figure being degraded by the noise generated in the following mixer stage.

Only gallium arsenide FETs can provide usable gain values at frequencies above 10 GHz. The main parameter of a GaAsFET that influences its microwave performance is the gate length. 1 μm gate length FETs can still provide about 6 dB of gain at 12 GHz with an associated noise figure of about 4 dB. 0.5 μm gate length FETs are much better – about 10 dB of gain can be obtained with a noise figure of about 2.5 dB. 0.25 μm gate length FETs are of course even better, but they are also very expensive and not yet regularly available on the market. The CFY 18 transistors, used in this project, are 0.5 μm gate length FETs packaged in the economical "micro-X" package and are manufactured by Siemens. Other manu-

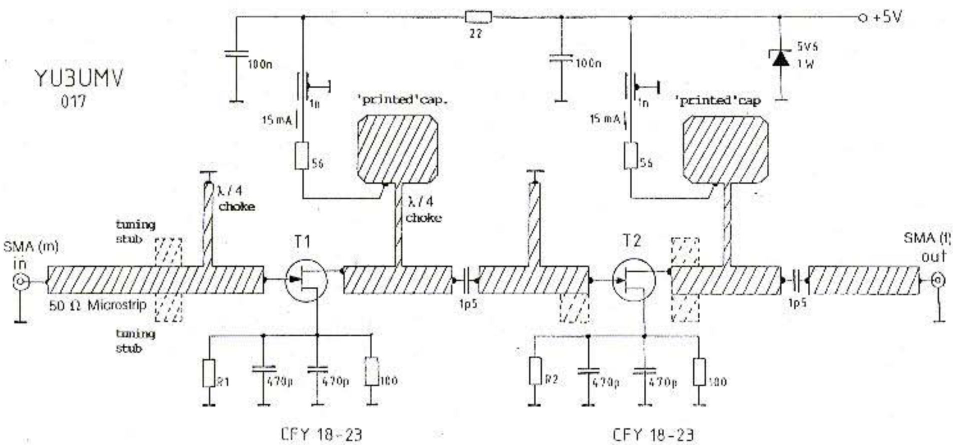
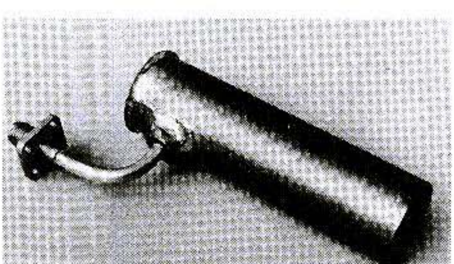


Fig. 3: Low-noise pre-amplifier for 10.95 to 11.7 GHz

facturers also supply similar transistors with similar microwave performances and at similar prices.

The parasitic reactances of a transistor package have a considerable effect on the transistor performance in the microwave frequency range. To improve the performances of their products, manufacturers usually try to use these unavoidable parasitics to partially compensate the parasitics of the transistor chip at least in the frequency bands where the transistor will most likely be used. It is therefore easier to match a packaged GaAs transistor in the 12 GHz frequency band than at frequencies below 2 GHz!



Photograph B: Tubular radiator without corrugated flange

The difference between optimum noise match and optimum gain match is small at 12 GHz – a CFY 18 matched for maximum gain will only show a 1 dB degradation of its noise figure. It is interesting to notice that the source reflection coefficients for optimum noise match and maximum gain match have a similar phase, the magnitude of the optimum noise figure match source reflection coefficient being much smaller than the maximum gain source reflection coefficient. The above is also valid for other similar transistors operating in the 12 GHz frequency range.

However, the specified transistor performance can only be obtained if the transistor is correctly installed into a suitable circuit. Almost all microwave transistors are packaged in cases suitable for installation into a microstrip circuit. At Ku-band frequencies only teflon-based laminates can be considered as substrate materials, since alumina, quartz and other suitable materials cannot be handled by amateur tools. The preamplifier is built on a 0.5 mm thick glassfiber-teflon laminate having an $\varepsilon_r = 2.33$ so that all the circuit elements have reasonable dimensions.

It is especially important to provide good source grounding / decoupling if the specified gain is to be obtained and other problems are to be avoided. Each FET has two source leads, each being bypassed by a leadless ceramic disc capacitor installed in a hole punched in the teflon laminate (**fig. 6**). Since these capacitors are made of high ε_r ceramic material, they behave practically as metal discs at Ku-band frequencies.

The two-stage amplifier uses a 50 Ω etched microstrip line and short capacitive tuning stubs made of thin copper foil to match the two FETs. The tuning is necessary since the transistors and the laminate have tolerances and the amplifier has to be matched to a real world antenna feed and to the following mixer stage, which are not ideal 50 Ω loads. A further advantage of this design approach is that the same printed circuit board pattern can be used between 10 and 13

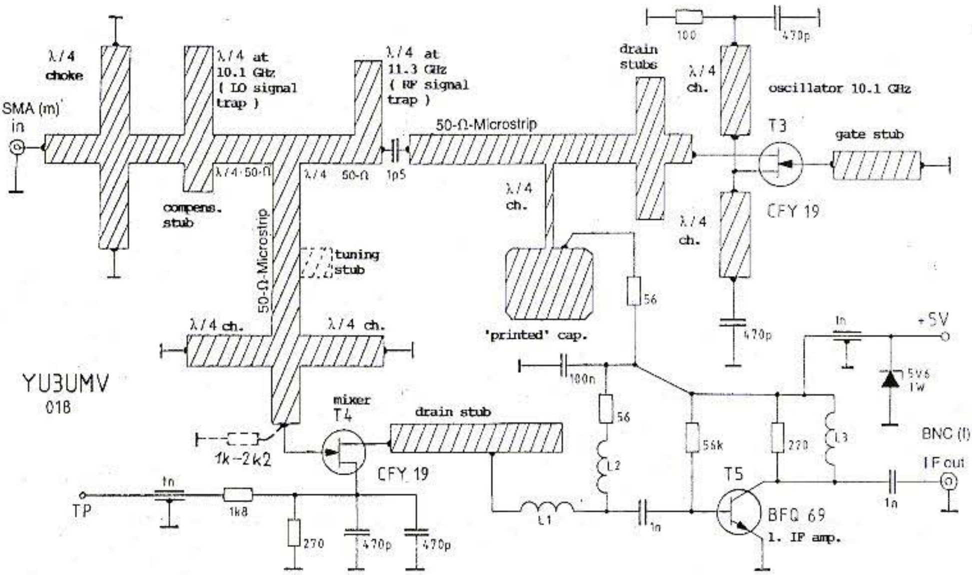


Fig. 4: Block down-converter module for 10.95 - 11.7 GHz / 0.85 - 1.6 GHz

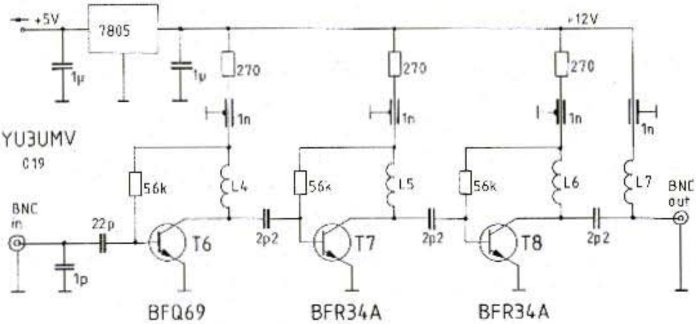


Fig. 5: IF Amplifier for 0.85 to 1.6 GHz and 5 VDC regulator

GHz by just repositioning the tuning stubs. The approximate positions of the tuning stubs for the frequency range 10.95 to 11.7 GHz are indicated in **fig. 3**.

The supply voltage is fed through λ / 4 chokes and is first bypassed by low-value "printed" capacitors so that low-frequency resonances of the supply network are dampened by 56 Ω resistors.

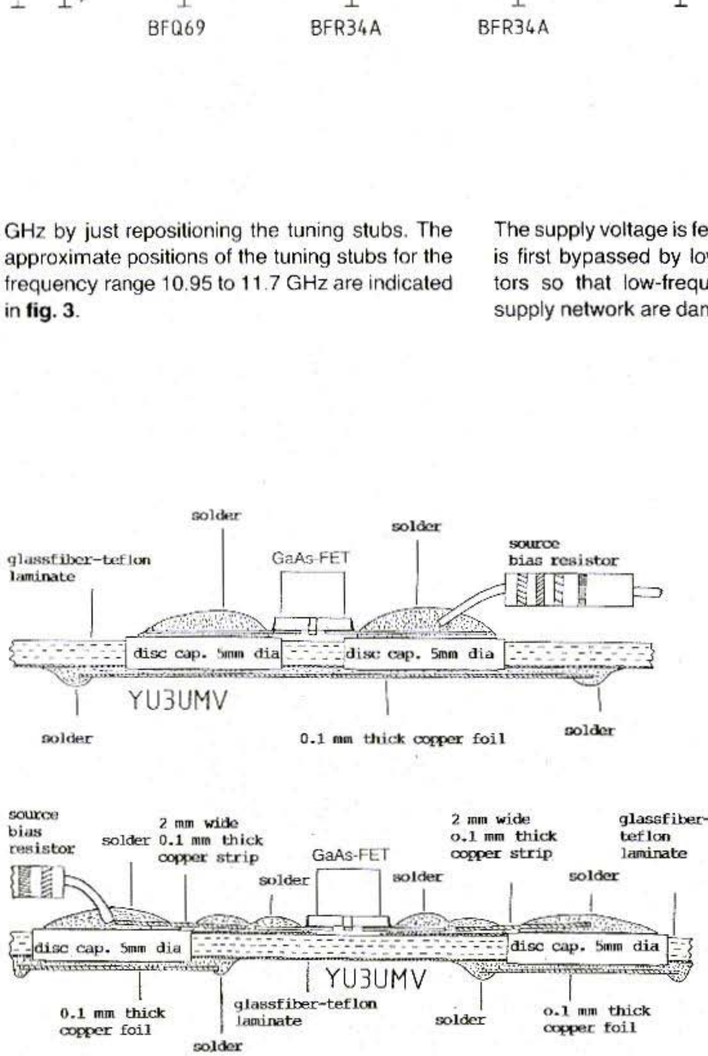


Fig. 6: Installation of the GaAsFETs and corresponding source bypass capacitors. Top: Installation of the amplifier / mixer GaAs-FETs (T 1, T 2 and T 4) Bottom: Installation of the oscillator GaAsFET (T 3)

If the amplifier is aligned to cover the 10.95 to 11.7 GHz band, it will provide about 22 dB of gain at the band center and about 18 dB at the band edges.

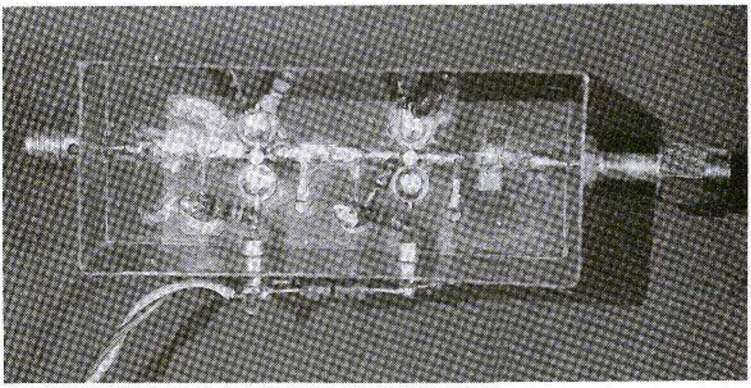
3.3. Block Down-Converter Module

Both silicon Schottky diode and GaAsFET mixers are practical at Ku-band frequencies. The advantages of a Schottky diode mixer are a low-noise figure, 6 to 8 dB, and little local oscillator drive power required – about 1 mW per diode. GaAsFET mixers, using 1 μm gate length FETs, achieve a slightly higher noise figure between 10 and 12 dB and require a higher local oscillator drive power, about 10 mW per GaAsFET. Unfortunately, the Schottky diode mixer noise figure also depends, to a large extent, on the noise figure of the IF amplfier used. The excellent noise figure specifications are usually obtained with narrow-band low-noise (1.5 dB) IF amplifiers. Since a satellite down-converter requires a broad-band IF amplifier (0.85 to 1.6 GHz), the noise figure of the latter can hardly be held below 5 dB across the whole IF bandwidth and the overall performance of a Schottky diode mixer approaches that of a GaAsFET mixer. On the other hand, a FET mixer has a small conversion gain and that is sufficient to make its noise figure almost independent of the following IF amplifier.

Packaged mixer diodes have high parasitic reactances that can hardly be tuned out over a wider bandwidth. On the other hand, beam lead diodes have only small parasitic reactances but are very difficult to handle due to their small physical size. Finally, a GaAsFET is actually cheaper and easier to use than a set of suitable diodes.

The block down-converter module, shown in **fig. 4**, uses a single-ended GaAsFET mixer in a grounded source configuration. Both RF and LO signals are applied to the gate of a 1 μm gate length FET (type CFY 19) and the IF signal is taken from the drain. Note that the actual square law-mixing process is actually a vertical process inside the FET structure and is therefore not dependent upon the FET gate length. The latter influences only the output IF signal frequency response.

To enhance the mixer performance, the gate network should have a low impedance for the output IF signal and the drain network should have a low



Photograph C: The low - noise pre - amplifier YU 3 UMV 017

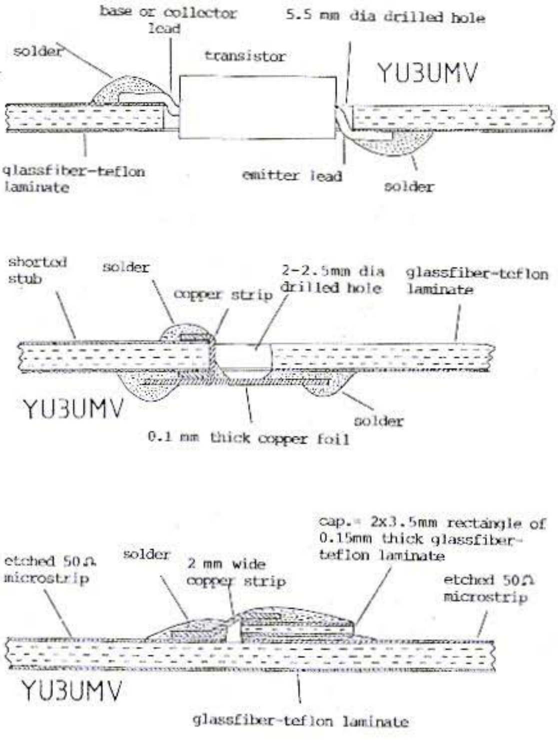


Fig. 7:
Top: Installation of the first IF amplifier transistor (T 5)
Middle: Grounding shorted stubs
Bottom: Installation of the 1.5 pF coupling capacitor

impedance for the input RF and LO signals. The gate network is a branching filter to couple both LO and RF signals to the mixer gate. The branching network uses tuned λ / 4 open stubs to reject the unwanted frequencies – the RF signal path includes a LO signal trap and the LO signal path includes a RF signal trap. The traps are located at λ / 4 from the branching point to reduce their influence on the desired signal paths. Four λ / 4 chokes are used to reject signals in the IF frequency range and provide a low, resonance-free impedance at the IF frequency.

The mixer drain stub operates in a 3/4 λ mode at RF and LO frequencies to enhance the conversion efficiency. For IF frequencies it behaves as a capacitor and builds, together with L 1, a low-pass filter and an impedance matching network to decrease the mixer output impedance.

The bandwidth, occupied by a frequency modulated TV signal transmitted through a satellite transponder, is usually between 25 and 36 MHz. A receiver frequency stability of a few MHz is therefore required and this can be met simply by a free running microstrip FET oscillator at 10.1 GHz. A 1 μm gate length GaAsFET CFY 19 can provide both the required stability and sufficient output power to feed the mixer stage.

To make a GaAsFET oscillate at frequencies around 10 GHz, an external feedback signal path has to be provided from the drain to the gate. Considering the S parameters of a packaged transistor this can be easily achieved by isolating the source leads from ground using two λ / 4 chokes. The oscillation frequency is mainly determined by the gate stub which operates in the 3/4 λ mode including the internal reactances of the transistor chip and its package. The drain stubs are required to provide a stable impedance in a wide frequency range and thus prevent oscillations at unwanted frequencies.

The supply voltage is fed through a λ / 4 choke and is bypassed by a "printed" capacitor as in the low-noise amplifier stages.

The block down-converter module includes an IF amplifier stage using a BFQ 69 silicon bipolar microwave transistor. The supply voltage for the mixer and IF amplifier stages is fed through IF chokes L 2 and L 3. Again, low-value resistors are being used to avoid parasitic resonances.

3.4. The 0.85 to 1.6 GHz IF Amplifier

The IF amplifier includes three stages equipped with silicon bipolar microwave transistors (see **fig. 5**). Since the gain of bipolar transistors decreases rapidly with increasing frequency in the low microwave region, the broadband IF amplifier should contain suitable networks to compensate the gain rise at low frequencies. A simple solution is to connect the collectors of the transistors to inductive loads (L 4, L 5 and L 6) and couple the signal to the following stage through a small capacitor. In this way, the amplifier will have a reasonably flat gain of about 25 dB in the band center and falling about 5 dB at band edges. If more gain is required, for instance to feed a longer cable to the indoor unit, T 7 and T 8 can be replaced by the better BFQ 69 type transistors, increasing the overall gain by about 5 dB. On the other hand, at least one stage can be deleted if the coaxial cable to the indoor unit is very short.

The IF amplifier receives the + 12 VDC supply voltage through the same coaxial cable from the indoor unit, decoupled by the choke L 7 and a feedthrough capacitor. The supply voltage of + 5 VDC for the GaAsFET equipped stages is obtained using a 7805 voltage regulator integrated circuit. Its input and output are bypassed by 1 μF multilayer ceramic capacitors to prevent unwanted oscillations.

The IF amplifier is not built on a printed circuit board, the components are directly installed into a suitable metal case. The 7805 voltage regulator IC is installed together with the two bypass capacitors on a small piece of unetched PCB laminate, which also acts as a cooling fin for the 7805. Note that, although the current drain at 5 V is below 100 mA, the use of a 1 A regulator in a TO - 220 package is recommended to avoid the thermal drift of the 5 V supply voltage and as a consequence, a drift of the 10.1 GHz oscillator!

4. CONSTRUCTION OF THE DOWN - CONVERTER

4.1. The Printed Circuit Boards

The low-noise RF amplifier and the block down-converter modules are constructed on two double-sided printed circuit boards made of **0.5 mm thick glassfiber-teflon laminate having an** ε_r **= 2.33.** The corresponding upper-side drilling plans are shown in **fig. 8**. The lower side should not be etched since it acts as a ground plane for the microstrip transmission lines. Other teflon laminates of thickness between 0.5 and 0.6 mm can also be used: the most standard ε_r = 2.55 laminate without any modifications, other lower ε_r laminates with just a slight re-positioning of the tuning stubs.

The teflon printed circuit boards have first to be carefully drilled as shown in **fig. 9**. Since teflon is a very soft material, only sharp (new!) drills are to be used at low speed. Small 1 mm diameter holes for the source bias resistors are not shown on fig. 9, in any case, these resistors can also be soldered to the walls of the case housing the circuit (**fig. 10**). The 100 nF bypass capacitor in the block

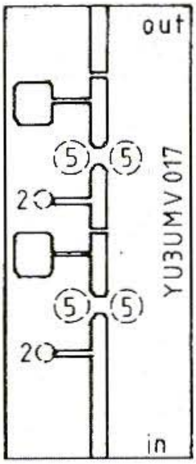


Fig. 8:
Drilling plan of the YU 3 UMV 017 PCB (Scale 1 : 1)

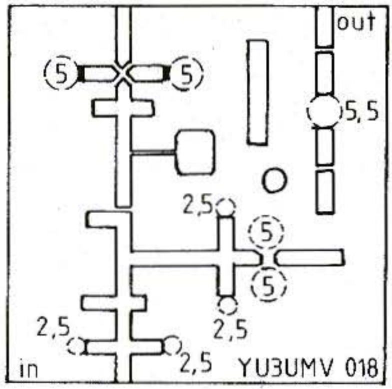


Fig. 9:
Drilling plan of the YU 3 UMV 018 PCB (Scale 1 : 1)

down-converter is installed in the center of the strip used as a support for the + 5 V supply. The other lead is of course grounded through a 1 mm diameter hole in the printed circuit board.

The λ / 4 chokes are grounded through 2 or 2.5 mm dia holes using small pieces of thin copper foil cut to the same width as the microstrips to be grounded and wrapped around the hole edge to provide the shortest possible grounding path. Then these holes may be tapped using small square pieces of tinned copper foil (**see fig. 7**).

The leadless source bypass disc capacitors should be pressed into the respective 5 mm dia holes. Both the copper cladding around these capacitors and the copper foil to be added should be well tinned to ensure good solder wetting and therefore a low grounding inductivity (**see fig. 6**).

The 1.5 pF coupling capacitors are small rectangles of thin teflon laminate as shown in **fig. 7**. Due to the small thickness of the insulation, these capacitors should be immediately checked for shorts after installation. At Ku - band frequencies, the virtual capacitive value of these capacitors is larger due to resonance effects.

The remaining components can now be installed. Of course the GaAsFETs will be installed last.

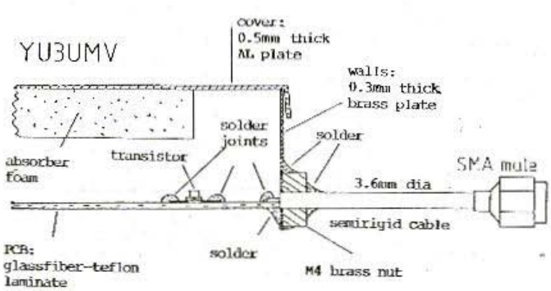


Fig. 10:
Installation of the PCBs

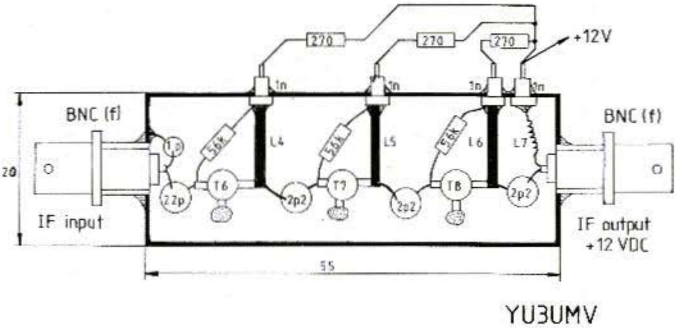


Fig. 11: Construction of the 0.85 to 1.6 GHz IF amplifier (YU 3 UMV 019)

GaAsFET manufacturers generally state that their product may be damaged by improper handling during installation due to electrostatic discharges through the very small area junctions. The handling procedures they suggest are, however, usually not very clever nor sufficient, to protect the delicate microwave semiconductors. Grounding oneself's body might be fatal for an operator if there is an accidental fault in the electrical installation of the laboratory!

Therefore I will describe here a simple and safe procedure, both for the GaAsFETs, and for the operator:

1. Work on an ordinary wooden table sitting on a wooden chair. Wood is an insulating material, however, its conductivity is sufficient to prevent the build-up of large electrostatic charges.
2. Disconnect the soldering iron from mains when soldering, even if you are using a separation transformer, since electrostatic charges are directly proportional to the capacities of the charged bodies.
3. Before each soldering operation, touch, with your finger, both the tip of the soldering iron and the ground plane of the printed circuit board to equalize the potentials.

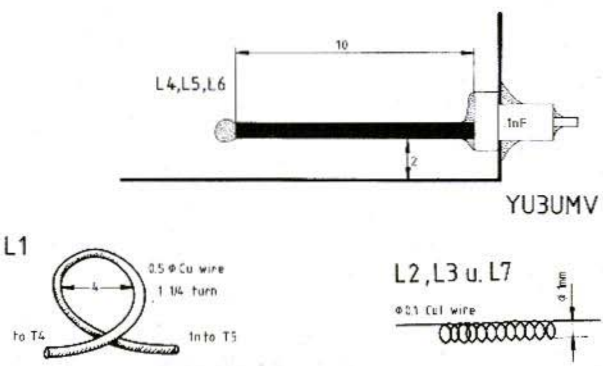


Fig. 12: Construction details of L 1 to L 7 in the YU 3 UMV 018 / 019 modules. Note that L 1 is soldered about 5 mm (λ / 4 at 11 GHz) from the open end of the mixer drain stub. L 2, L 3 and L 7 are IF λ / 4 chokes. Total wire length = 65 mm. The exact number of turns (about 10) is not important. L 4, L 5 and L 6 are straight lines soldered between the transistor collector terminals and the feed-through capacitors.

Following these simple rules I have not yet destroyed a single GaAsFET although I have soldered more than twenty GaAs transistors during the developement of the described down-converter. Many of these have even been soldered several times as the original prototypes did not work satisfactorily. Of course any soldering operation should only be done with the DC power switched off and the circuit disconnected from other circuits and / or test equipment. Electrical equipment that produces induced charges, like CRT displays, induced voltage or current spikes, should also be switched off during the installation of GaAsFETs.

Following the assembly the low-noise amplifier printed circuit board can be immediately installed in a suitable metal box as shown in **fig. 10**. The block down-converter printed circuit board should be first roughly aligned, especially the oscillator frequency, before installation in a suitable metal case. The walls of the housing are 22 mm wide strips of thin brass plate, the cover is made from 0.5 mm thick aluminium plate and the bottom is the same printed circuit board. Feedthrough capacitors are soldered into holes made in the walls of the metal case. The 5 V 6 / 1 W overvoltage-protection zener diodes are installed externally. Each module requires its own zener diode since voltage spikes can also be induced in the 5 V supply wiring, for example, due to accidental short circuits.

A piece of absorber foam should be installed below the cover to dampen the unwanted parasitic resonances of the housing.

Ku-band frequencies require SMA connectors. SMA connectors are usually used together with short lengths of 3.6 mm Ø semirigid cable. To increase the mechanical strength of the assembly a M 4 brass nut is screwed onto the cable end and then soldered to the case. The internal diameter of the M 4 thread has to be slightly enlarged with the aid of a small round file to fit the outer jacket of the semirigid cable. If suitable SMA connectors are available these can also be directly soldered onto the case.

BNC connectors are suitable for the IF frequency range between 0.85 and 1.6 GHz. Female BNC connectors can be directly soldered onto the metal cases as shown in **fig. 11**.

The components of the IF amplifier are installed in a 55 mm long, 20 mm wide and 15 mm high box made of thin brass sheet (**see fig.11 and fig. 12**).

4.2. Components for the Outdoor Unit

4.2.1. Pre-Amplifier YU 3 UMV 017 Component List

T 1, T 2:	CFY 18 - 23 (Siemens)
Z diode:	ZPD 5V6 (5.6 V / 1 W)

4 x 470 pF (approx.) disc caps: leadless, 5 mm dia for punched-out hole fitting
2 x 1.5 pF (approx.) caps:
made from 2 mm x 3.5 mm x 0.13 mm teflon-glassfiber PCB material, double-sided
2 x 1 nF (approx.) feedthru caps (short form), solder-in types
2 x 100 nF ceramic decoupling caps

All inductors are etched!

Carbon film resistors in form 0204 (2 mm dia, 4 mm long)

1 x	22 Ω
2 x	56 Ω
2 x	100 Ω
R 1, R 2:	50 - 220 Ω (see text)

SMA coax. connectors:
1 x plug
1 x panel socket

4.2.2. Converter YU 3 UMV 018 Component List

T 3, T 4:	CFY 19 (Siemens)
T 5:	BFQ 69 (Siemens)
Z diode:	ZPD 5V6 (5.6 V / 1 W)

4 x 470 pF (approx.) disc caps: leadless, 5 mm dia for punched-out hole fitting

1 x 1.5 pF (approx.) cap:
made from 2 mm x 3.5 mm x 0.13 mm teflon-glassfiber PCB material double-sided
2 x 1 nF ceramic caps
2 x 1 nF (approx.) feedthru caps. (short form), solder-in types
1 x 100 nF ceramic decoupling cap.

L 1 **see fig. 12**:	approx. 5 mm (λ / 4 at 11 GHz) soldered away from the open end of the mixer drain stub
L 2, L 3 **see fig. 12**:	coil length = 65 mm, (λ / 4 at IF) 10 turns (approx.), uncritical

Carbon film resistors in miniature form (0204):

2 x	56 Ω
1 x	100 Ω
1 x	220 Ω
1 x	270 Ω
1 x	1 k 8
1 x	56 k
1	SMA cable connector
1	BNC panel socket

4.2.3. IF Amplifier YU 3 UMV 019 Component List

T 6:	BFQ 69 (Siemens)
T 7, T 8:	BFR 34 A (Siemens)
1	7805 (5 V regulator)

Ceramic disc caps.:

1 x	1p
3 x	2 p 2
1 x	22 p
2 x	1 μF / 16 V tantalum electrolytic
4 x	1 nF (approx.) feedthru caps. (short form), solder-in types
L 4, L 5, L 6:	straight, silvered wire, 1 mm dia, soldered according **fig. 12** between collector connector and feethru cap.
L 7:	total length = 65 mm (as L 2 and L 3)

Carbon film resistors in form 0204:

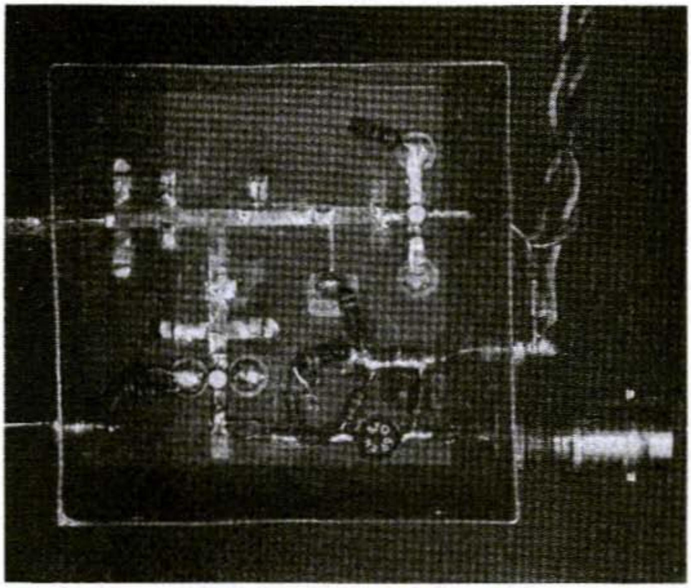
3 x	270 Ω
3 x	56 k
2 x	BNC panel sockets

5. ALIGNMENT AND TESTING OF THE DOWN-CONVERTER

There are many different possible alignment procedures depending on the instrumentation available. Since most amateurs only have little microwave instrumentation available, an alignment procedure that requires a minimum amount of professional instruments will be shown, using simple home-made instruments such as a wideband noise generator and equipment an amateur may be expected to have, such as a 1296 MHz converter and a receiver with a disconnected AGC for noise figure / gain measurements.

The three-stage IF amplifier does not require any adjustment. Reasonable values of DC currents (around 15 mA) flowing through the transistors T 6, T 7 and T 8 already ensure that the amplifier is operating correctly. The + 5 VDC voltage regulator should also be checked before connecting the two modules with GaAs transistors.

The block down-converter module should now be connected. The operation of the 10.1 GHz FET oscillator should be checked and the frequency aligned to the desired value. When T 3 is oscillating correctly, its current drain should be around 15 mA (to be measured as a voltage fall on the source bias resistor). Touching the drain and gate stubs at the same time with your finger should stop it oscillating and the current drain should fall to about 10 mA. If similar values are not obtained (tolerances of ± 20 % are allowed) then the value of the nominally 100 Ω source bias resistor should be modified. Note that a wide spread



Photograph D: The converter YU 3 UMV 018

of the transfer curve $I_{DS} = f(U_{GS})$ is normal for GaAs transistors.

The frequency of the oscillator can be adjusted by the T 3 gate stub length. As etched on the teflon printed circuit board, this stub is slightly too long and the oscillation frequency is generally 300 to 400 MHz too low. The grounding strip should be carefully removed and the gate stub shortened using a small file producing a 3 mm wide cut in the laminate. Since the gate of the FET is not connected during this operation, observe all the handling precautions taken when soldering the GaAsFETs. The gate stub should be shortened by about 1 to 1.5 mm to obtain 10.1 GHz. Fine frequency corrections can be made by a small capacitive tuning stub – a small piece of thin copper foil soldered about in the center of the gate stub.

Unfortunately, it is not easy to measure the frequency of the local oscillator with amateur instruments. The ideal solution is a spectrum analyzer or a sensitive microwave frequency counter connected to the input of the module. If the signal is not sufficient, then the LO trap resonator has to be temporarily detuned, but this will also shift the oscillator frequency by about ± 50 MHz. Alternatively, a Schottky-gunn module, well known from the early amateur microwave activity, can be used to down-convert the FET oscillator signal to the VHF / low UHF range where it can be monitored easily. Even the famous Lecher wires, although spaced by 1 cm, are still very accurate at 10 GHz, but a cheap and sensitive detector is not readily available. Absorption resonators are also accurate, but they too, need a sensitive detector.

Actually, it is sufficient to bring the oscillator frequency to within ± 50 MHz, fine adjustments can be done later. The block down-converter printed circuit can now be installed in a suitable case as shown in **fig. 10**. The voltage on the source of T 4 (mixer transistor) should now be checked on the mixer test point. With the LO drive signal applied, the current through T 4 should be within 7 and 10 mA to obtain the best mixer noise figure. Disabling the oscillator, as described earlier, the T 4 source voltage should fall by about 500 mV. The source voltage increase in an active FET mixer, when applying the LO drive signal, has precisely the same meaning as the rectified current of diode mixers: it does provide an insight into the non-linear mixer operation and an estimate of the mixer efficiency.

The mixer and the low-noise amplifier should now be aligned for the maximum available gain in the desired frequency band between 10.95 and 11.7 GHz. A simple noise generator can be used as the signal source. An inversely polarized B - E junction of a BFQ 69 transistor is a simple and efficient noise source; at 12 GHz it can supply over 30 dB ENR with a zener current of about 5 mA. Since many suitable designs were already published in VHF Communications, and in other magazines, the construction of a noise source will not be discussed here.

If a noise generator is being used as the signal source, a sensitive receiver is required to detect the signal at the IF output of the block down-converter module. A suitable IF is 1296 MHz since it falls almost in the center of the IF passband 0.85 to 1.6 GHz and converters are readily available for this frequency. The 1296 MHz converter should be connected to a (possibly wideband) receiver, equipped with a linear detector and with the AGC disconnected. A noise figure measurement receiver is ideal for this purpose. Of course, the receiver should be equipped with a manual gain control (attenuator) to adjust the signal level to obtain a suitable output indication on the S meter.

If a wideband noise generator is used as a signal generator, care should be taken not to tune the low-noise amplifier and the block down-converter to the image frequency. A fool-proof solution is to build two horn feeds (see fig. 2, the corrugated flanges are not yet necessary). One horn is connected to the input of the low-noise amplifier or block down-converter to be aligned and the other is connected to the output of the noise generator. The lowest cutoff frequency of the waveguide (mode TE_{11}) is around 9.75 GHz for the given internal diameter of the horn. This is, of course, below the wanted frequency range 10.95 to 11.7 GHz but above the image frequency range 8.5 to 9.25 GHz. Therefore the horn feed is a simple and very efficient image rejection filter.

The noise generator signal level can easily be adjusted by the distance between the two horn apertures. The low-noise preamplifier can be tuned to the actual horn feed impedance since the overall system noise figure is the only important parameter.

First of all, the adjustment of the block down-converter module alone should be completed. If suitable instrumentation is available, the LO signal trap should be tuned for minimum LO leakage at the input connector. Otherwise, it should not be touched since it has already been etched very close to the required dimensions. Then, the noise generator signal should be fed to the input, as described above, and the position of the tuning stub should be found. The tuning stub is a small piece of copper foil, about 2 x 3 mm^2, and is to be moved along and across the 50 Ω microstrip using a thin rod of insulating material and finally soldered in the position that gives the maximum conversion gain. This operation may shift both the oscillator frequency by a few tens of MHz and slightly increase the voltage at the mixer test point. However, both these effects have almost no influence on the performance of the converter.

Now the low-noise amplifier can be inserted between the horn feed and the block down-converter module. The source bias resistors should be adjusted to obtain a drain current of about 15 mA. Without any tuning, a gain of 12 to 14 dB can be expected from the S parameters of the transistors. Firstly, the interstage match should be optimized for maximum gain. Then the output match should also be optimized for maximum gain. Finally, the position and length of the input tuning stubs for the maximum gain should be found. The input tuning stubs are, however, not yet soldered in this position, since we actually require the optimum noise match. This can simply be obtained by leaving the tuning stubs in the same position but shortening them to get 1 to 2 dB less gain. Alternatively, the effect of a tuning stub can be decreased by bending up the open end of the copper foil.

The CFY 18 transistors are selected by the manufacturer according to the noise figure indicated by two numbers. The CFY 18 - 23 selection is specified to have a 2.3 dB noise figure at 12 GHz. Considering the contribution of the following stages, a 3 dB noise figure is the theoretical minimum. Various losses between the horn feed and the first transistor will increase the noise figure to about 4 dB in the band center and a few decibels more at band edges. The above estimate was found to be in good agreement with practical carrier to noise ratio measurements on satellite signals, taking into account the satellite EIRP, the free space insertion loss and the receiving antenna gain.

A tuned low-noise amplifier has some selectivity. This is useful to prevent the noise figure degradation due to amplifier noise in the image frequency range, since the mixer input network is not very selective. On the other hand, sometimes it may be necessary to optimize the alignment later to cover the whole 10.95 to 11.7 GHz band better.

Of course, the waveguide horn feed provides a very high image rejection if the waveguide is not too short. Although the length of the waveguide horn is not critical, 70 to 80 mm is a practical value.

5.1. Modifications

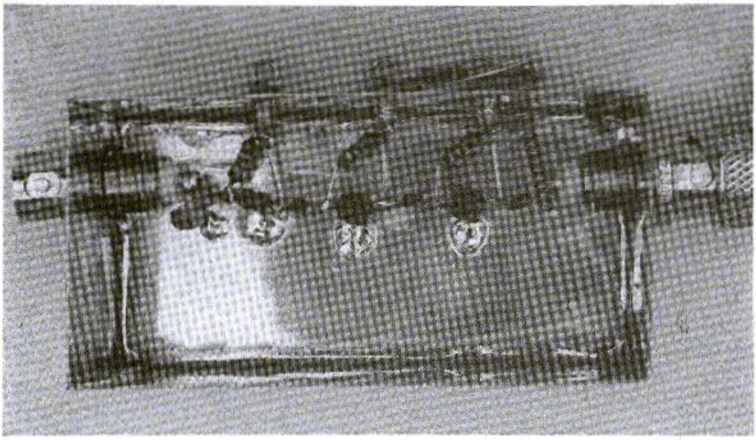
Although the described low-noise down-converter was designed for the 10.95 to 11.7 GHz segment, it can be tuned for almost any Ku-band satellite downlink segment. The IF frequency band can hardly be changed, the choice 0.85 to 16 GHz representing the best compromise considering available semiconductors, reasonably priced cables, connectors and standardized indoor units. The oscillator frequency has to be tuned to the required value first (by adjusting the gate stub length). The drain stubs should not be shortened by more than 1 mm each otherwise there is danger of parasitic oscillations in the 8 to 9 GHz range. Now the LO signal trap should be adjusted, then the RF signal trap and finally, after positioning the tuning stub, the short compensation stub should be corrected. The low-noise amplifier can be adjusted in the same way as explained earlier, however, the positions of the tuning stubs will be quite different from those indicated in fig. 3.

As a practical experiment, I have tuned a prototype for the 12.5 to 12.75 GHz frequency band to receive the two French TELECOM 1 A and 1 B satellites. Besides a slightly lower gain, due to the higher frequency of operation, no other problems were noted. of course, the horn feed had to be redimensioned – a 16 mm inner diameter tube was used, the probe length was reduced to 4.7 mm while the spacing from the shorted waveguide end remained 12 mm (see fig. 2).

A number of manufacturers actually supply suitable GaAsFETs, both 0.5 μm gate length and 1 μm gate length types with similar S parameters as the CFY 18 and CFY 19 types. Although these were not yet practically tried, no major problems should be expected except for the obvious repositioning of the tuning stubs. Of course, the FETs should be packaged in suitable microwave packages. Ceramic packages still offer a better performance to price ratio then plastic packages, which are also more sensitive to improper handling and high temperatures encountered during the soldering operations.

5.2. Conclusion

Ku-band down-converters for small satellite television receive stations are already a standard product on the professional equipment market.



Photograph E: The IF amplifier YU 3 UMV 019

These down-converters usually use the same IF band, generally between 900 and 1700 MHz (+/−100 MHz). The input connector at Ku-band frequencies is a waveguide flange and a suitable horn feed is usually supplied separately. To increase the effect of the feed mismatch on the noise figure of the low-noise preamplifier, a low-loss circulator with one port terminated with a matched load (isolator) is usually inserted between the waveguide to microstrip transition and the first amplifier stage. A circulator is a difficult to get and an expensive item but fortunately, in amateur conditions, each converter can be individually aligned and a small degradation of its performances will only be noticed at band edges.

Professional Ku-band down-converters also use oscillators stabilized with dielectrical resonators. These are some orders of magnitude more stable than the free running oscillator shown in this article. Such a high stability is required in cable television headend stations, where a number of receivers must operate unattended reliably for months. An amateur receiver is usually hand-tuned and any down-converter drift can immediately be corrected. In practical use it was difficult to notice this instability, since it follows the ambient day / night temperature cycle while the receiver was usually tuned from one channel to another much more frequently. The receiver was **not** equipped with an AFC circuit!

All the Ku-band down-converters have a fixed-tuned local oscillator and convert at the same time the whole Ku-band segment down to the relatively wide IF frequency band. A tunable down-converter would be a better technical solution for single channel reception, however, it seems that suitable components, to build Ku-band VCOs, are not readily available.

Although the antenna gain and the down-converter noise figure are considered the most important parameters of a satellite receiving station, the performance of the IF circuits, and in particular the wideband FM demodulator, is equally important. Amateurs usually only have small antennas. Regardless of the size of the available antenna, there will always be some signals at the margin of the system sensitivity. Since the satellite wideband FM video signal contains a lot of redundancy, it is possible to extend the threshold of a FM demodulator even beyond the theoretical values. Therefore a suitable IF tuner / demodulator, usually referred as the indoor unit, will also be described in a future article, including a threshold extension demodulator adaptable to different signal-to-noise ratios, a tunable audio IF to re-

s used and of course a
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ECAM TV set.

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Jochen Jirmann, DB 1 NV

Voltage - Controlled Tuned Wideband Oscillators

For many measurements frequently undertaken in amateur practice, such as the tuning of filters or antennas, a signal source is required which is capable of being tuned to the limits of the amateur band concerned and beyond it. If a commercial sweep generator is not available, a suitable sweep oscillator can be made without too much difficulty. This article should help to dispel the myth of a black art surrounding this type of circuit by explaining the techniques involved and also assist in its construction.

1. INTRODUCTION

The usual practice in amateur equipment is to try and limit the tuning range of the voltage - controlled oscillator (VCO) of the synthesizer as much as possible, in order to mitigate the unavoidable effects of the high oscillator noise pedestal and the not negligible effects of the tuning voltage noise. Suitable circuits have appeared in various publications and the work of DJ 7 VY is well known in this area. In amateur test practice, oscillators are required which can be tuned over a large bandwidth, whether it be to determine the impedance of wideband antennas, the tuning of harmonic filters etc. or as a local oscillator in a superhet receiver. This article will introduce a few circuits which may be employed as wideband VCOs and which will substitute for many of the purposes for which a commercial sweep generator is used.

The author would like, in particular, to encourage the reader to make some experiments as the test equipment required is held to reasonable limits. Two 12 V DC power supplies are required together with a 0 - 30 V variable supply. An RF power meter (or at least a power indicator) and a frequency counter should complete the list of equipment necessary. If a UHF counter is not available, an ECL prescaler such as those found in TV tuners, costing about DM 20, may be added to the counter thus extending its range from 10 or 20 MHz into the region of 1 GHz. Suitable types are e. g.: The Telefunken U 264 / U 664 (divide by 64), the U 666 (divide by 256) or the Siemens SDA 2211 (divide by 64). There are many circuits in amateur publications which deal with the way in which the decimal point may be inserted at the correct point on the indicator read-out following the addition of the prescaler. If the exact tuning voltage for a particular frequency is desired to be known, then a digital voltmeter will also be necessary.

In order to keep the parasitic reactances to as low an order as possible, the conventional printed circuit board techniques must be dispensed with. Instead coupling and blocking disc capacitors, using components without wire connections, the circuits are soldered directly to the ground plane or circuit tracks of the PCB. They are also used as support tags for other components. The photographs of **fig. 3** show that disc ceramics can be soldered directly to the walls of tin-plate screening boxes as well as on PCB copper. In order to ensure a high Q in tuned circuits, it will always be preferable to employ ground areas made from copper or silver coated copper. A suitable preparation should also be used to counter the effects of copper oxidation and solder flux corrosion.

2. COMPONENTS

Professional wideband techniques mostly employ YIG oscillators whose frequency determining element consists of a chip of yttrium-iron-garnet. The intrinsic frequency of the YIG chip can be varied over a few frequency octaves by the application of an external magnetic field.

When such components became too expensive for amateur purposes, a substitute had to be found. The basic requirements for the family of oscillators described here ar as follows: –

- Frequency range of interest from 100 MHz to 1 GHz
- Each oscillator must tune over a band of 0.5 to 1 octave
- Output power of greater than 1 mW
- Tuning voltage 0 to 30 V
- Output power variation over tuning range: less than 6 dB
- Harmonic content: less than 20 dB
- Where possible a buffer stage should be incorporated

Narrow-band oscillators may be readily use barrier FETs to deliver particularly noise-free signals. FETs have, however, the disadvantage that they possess a relatively large input capacitance (5 pF) which lies directly across the frequency determining resonant circuit, effectively limiting the tuning range. The transconductance of FETs, in relation to bipolar devices, is relatively small and therefore the effects of this input capacitance cannot be reduced by looser coupling to the tank circuit.

Bipolar transistors, on the other hand, have an output capacitance of under 1 pF and are, in spite of their worse noise characteristics, more suitable for wideband oscillators than FETs. Experiments have shown, moreover, that a transistor having a higher transit frequency performs no better, in this application, than one which only just meets the frequency specification. In general, it is sufficient to choose a transistor which has a transit frequency of 1.5 to 2 times the intended working frequency of the circuit. In television tuners, working below 1 GHz, the preferred PNP oscillator transisstors are as usually those such as the BF 970, and BF 979. Above 1 GHz the low-cost BFW 92 and the BFR 90 have proved well suitable. In any case, suitable transistors may be found by experimentation and it is surprising that many are to be found in the ranks of "general purpose transistors".

In all wideband oscillators, a careful control of parasitic oscillations, arising in coupling and tank circuits, must be undertaken as these lead to unpredictable tuning characteristics. The control of parasitic oscillations is always more difficult as the frequency increases. All circuits are therefore designed so that the tuned circuit is grounded on one side and the oscillator supply voltage can be directed via this to the active device. This avoids the use of the critical radio frequency choke (RFC) in the collector and non-critical resistors may be employed both to set the transistor working point and for decoupling purposes. PNP transistors allow a particularly simple form of construction using a positive supply voltage.

In the frequency range 500 to 1000 MHz, normal UHF tuner diodes, such as the BB 105, BB 505 or similar, may be used. They offer a tuning capacitor ratio of about 5 which ensures an octave coverage providing that the resonator tuned circuit capacitance is kept low.

At lower frequencies, the hyperabrupt types used in cable TV tuners, such as the BB 609, are suitable. These have a capacitance ratio of 13 which allows a tuning range of 2.5 to 1 to be possible. As the Q of these diodes is quite low in the UHF region, they should not be employed higher than 300 MHz.

The UHF diodes around 1 GHz and above, which have plastic or glass encapsulation, are hardly usable owing to a series inductance of some 3 nH. The self-resonance of a BB 105 lies, according to the barrier voltage, between 750 MHz and 2 GHz. Surprisingly, they have been employed in the latest UHF tuners in the form of MiniMELF diodes for surface mounting. The Intermetall BB 621, owing to its construction and low series inductance, has a very good Q at frequencies over 1 GHz. The following examples of circuits will show that this diode may be employed in circuits up to 2 GHz.

3. BASIC CIRCUITS

The choice of suitable oscillator circuits which, with very little alternation, are able to be used on the various frequencies of interest, is all that remains. There are two basic oscillator principles which come into consideration, the two-terminal and the four-terminal oscillator circuits. The four-terminal oscillator uses the transistor as an amplifier and connects input and output together via a tuned circuit. The two-terminal oscillator uses the transistor as a negative resistance which counters the losses in the tuned circuit. This type of circuit works as well at very high frequencies because the transistor's internal capacitance is used as part of the feedback mechanism.

Now that the basic types have been explained, a few examples of circuits for various frequency ranges will be introduced.

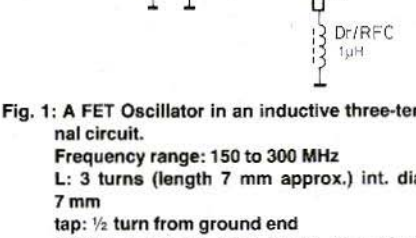

Fig. 1: A FET Oscillator in an inductive three-terminal circuit.
Frequency range: 150 to 300 MHz
L: 3 turns (length 7 mm approx.) int. dia = 7 mm
tap: ½ turn from ground end
Output coupling: loop about ½ turn from ground end

4. PRACTICAL CIRCUITS

4.1. A FET Oscillator for Frequencies up to 300 MHz

The circuit of **fig.1** shows a tapped inductor circuit with the BF 256 FET connected in a drain driven manner. As the input capacitance of the FET is in the region of 5 pF, a tuning range of only one octave is possible despite the use of a hyperabrupt varicap diode.

An important circuit detail is the capacitor phase shifter C 1 connected between the source and the DC blocking and as the FET operates as a source follower the input voltage at the gate and the output voltage should be in phase. At the frequency under consideration i. e. above 100 MHz, this assumption is no longer valid and the source voltage phase shift must be compensated by using a (too) small coupling capacitor. Owing to the large range to be covered, the value of this capacitor must be only a compromise chosen on the basis of the output power remaining reasonably constant over the tuning range. It is possible to employ another varicap here in order that the feedback phase shift compensation may vary with frequency. This idea was not persuad in the interests of developing a circuit which would be readily reproducible.

This circuit is only intended for applications where

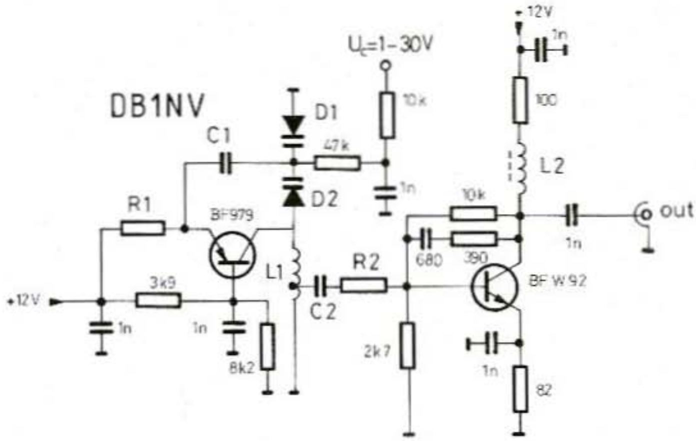

Fig. 2:
An 80 to 1000 MHz bipolar oscillator, components as in table 1

a really noise-free signal is required and where the tuning range need not be too large. The oscillator of **fig. 2** was dimensioned for a frequency range of 150 to 300 MHz.

The following bipolar oscillator is intended for universal application at frequencies between 80 and 1000 MHz in three bands. With a curtailment in performance it may be made to operate at frequencies up to 1.3 GHz.

4.2. A Bipolar Oscillator for 80 to 1000 MHz

The oscillator shown in **fig. 2** represents a capacitive three-point circuit which does not require a tapping on the oscillatory tuned circuit in order to sustain oscillation. The transistor, a PNP BF 979 or BF 479, works in a commonbase circuit with the collector being effectively at ground potential with the tuned circuit.

Frequency range	R 1	R 2	C 1	C 2	L 1	L 2
80 to 200 MHz	390	39	68 p	47 p	7.5 turns, 4 mm Ø F 100 - core tapped near ground end	choke 33 µH
200 to 500 MHz	390	120	22 p	47 p	3.5 turns, 4 mm Ø length approx. 8 mm, tapped near ground end	choke 22 µH
500 to 1000 MHz	220	22	6p8	2p2	strip 15 x 3 and 3 mm above ground, tapped 3 mm from ground end	choke 4.7 µH

Table 1

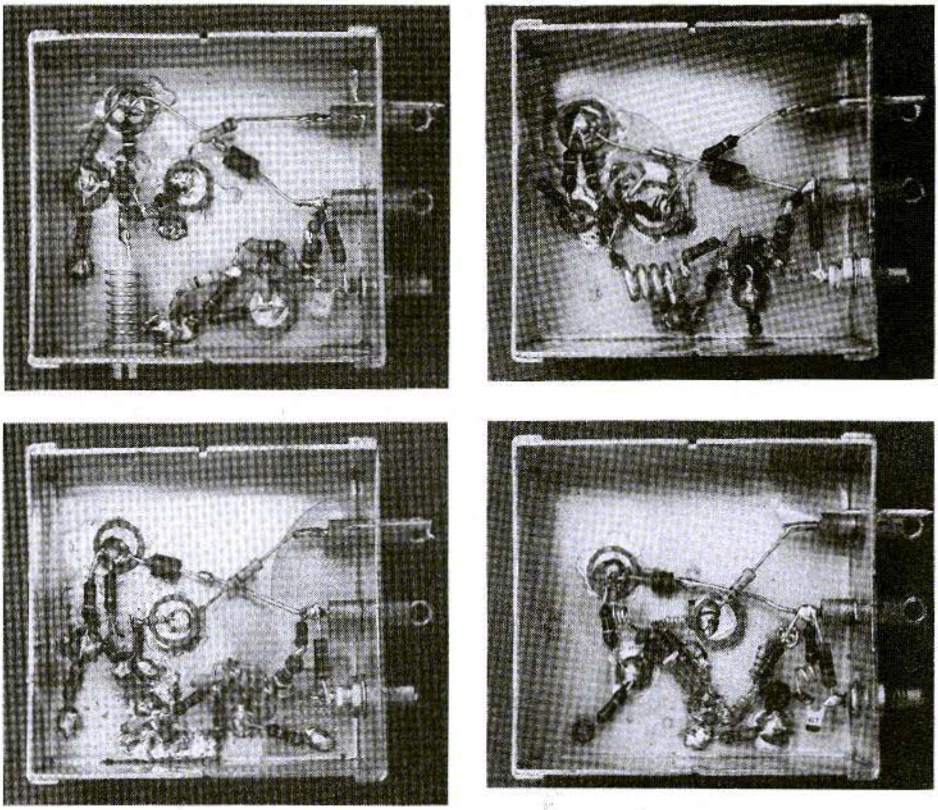

Fig. 3: The author's prototype constructions

The capacitive divider forming the feedback circuit is composed of two varicap diodes together with the coupling capacitor C 1. The latter also compensates for the phase shift through the transistor.

The frequency determining circuit has an air-cored coil inductor for the frequency ranges 80 to 200 MHz and 200 to 500 MHz and a conductive strip inductor supported above the PCB plane for the range 500 to 1000 MHz. The tapping on the tuned circuit inductor controls the degree of coupling to the buffer stage which, in turn, affects the degree to which the oscillator frequency is pulled by HF output load variations. The tapping point also affects the bandwidth, the Q and therefore the harmonic content as well as the output level. If a low harmonic content is required, the coupling must be kept very low i. e. the tapping point near the earthy end of the inductor in order that the buffer stage is not driven too hard.

The important characteristics of the oscillator are summarized in **table 1** and the photograph of **fig. 3** shows the prototypes constructed by the author for the bands 80 to 200, 200 to 500, 500 to 1000 and 1000 to 1350 MHz. The last oscillator will not be mentioned further here because it represents the highest frequency possiblle with this type of circuit. The oscillator could be dimensioned for the range 30 to 80 MHz by merely increasing the size of the air-cored inductor. The tuning capacitance and self-capacitance should, however, be held to low levels in order that the varicap is able to cover the desired sweep range. The frequency can be further reduced by using medium-wave type varicaps (C = 20 to 500 pF). The constructor should note that the various resistance and capacitance values are changed according to the frequency range of interest. In particular, the high frequency example 500 - 1000 MHz should be constructed with the shortest possible RF leads and the layout, shown in the photograph, closely followed.

4.3. Oscillators for the Range 1 to 1.5 GHz

In order to construct VCOs for frequencies higher than 1 GHz, a few decisive circuit alterations were necessary. Firstly, the varicap diodes were replaced by a better type (BB 621). The inductive part of the tuned circuits was too small, physically, to be constructed from strip line (L < 10 mm) and had to be made from $\lambda / 2$ resonators, this doubles the length thus making it more manageable. The one end of the resonator line has a varicap diode tuning and the other end has a trimmer to set the lower limit of the frequency range tuning. The upper frequency limit is determined by the residual capacity of the varicap diode. The overall frequency range of this oscillator is not as great as the other versions described earlier, having only a half octave span.

Older readers will, perhaps, be aquainted with the tank circuit of the first tube UHF power amplifiers. The transistor has an earthed collector and driven at HF to a floating emitter. Owing to the transistor's internal feedback via the base-emitter capacitance, it has at the base, as far as HF is concerned, an input resistance having a negative real component which decreases the loading across the tank circuit.

Using a small capacitance, of a fraction of a picofarad at the emitter, this feedback can be optimized. The capacitor can take the form of a 0.5 to 1 cm wire bent to a suitable position above ground.

The HF is coupled out from the base circuit by means of a trimmer. A buffer stage was not used owing to its difficult design and the fact that its effect is not particularly good due to the isolation from output to input of a 1 GHz, simple transistor stage being very small. The use of a circulator was not contemplated on grounds of cost.

The 1 to 1.5 GHz oscillator of **fig. 4** is shown, in prototype construction, in the photograph of **fig. 5**. An experimentally built oscillator, covering 1.7 to 2.4 GHz, displayed a large output power fluctuation when tuned over the range together with poor tuning characteristics and frequency jumps. This, evidently, is the frequency limit for oscillators built with standard components. Expensive glass tubular trimmers are not absolutely necessary for frequencies under about 1.5 GHz, the cheaper teflon-foil ("Sky") trimmers may be

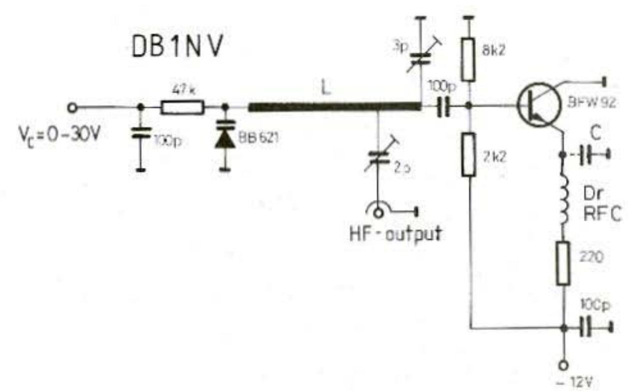

Fig. 4: A 1 to 1.5 GHz oscillator

Fig. 5:
The 1 to 1.5 GHz oscillator prototype

substituted. Further attempts to increase the frequency of this type of oscillator to 3 GHz, by reducing the tank circuit to 5 mm, was not encouraging. Besides the output power varying over the tuning range from 0.1 to 10 mW, there was a tendency to mode-jump, hysteresis effects and similar misfortunes.

4.4. A GaAs-FET Oscillator for 1 to 1.6 GHz

After the GaAs-FET, such as the CFY 13, became cheaply available to the radio amateur, it has become possible to use them in the construction of broadband VCOs. As **fig. 6** shows, this circuit is very similar to that of the preceding bipolar oscillator but the resonator is tuned at both ends with varicap diodes. This is facilitated because of the very low load on the resonator imposed by the FET. The HF coupling is carried out by means of a small loop located near a current antinode in the tank circuit. The additional feedback coupling, using the 1 pF capacitor, improves the oscillator starting characteristics at the low end of the frequency range. The drain resistor damps any tendency to parasitic oscillation in the SHF range. The power output of 1 to 2 mW over the range from 1 to 1.6 GHz was achieved with this circuit.

5. OBSERVATIONS

In all probability, the first experimental oscillator will not behave quite as well as expected. The following information notes should help to sort out a few possible sources of error: -

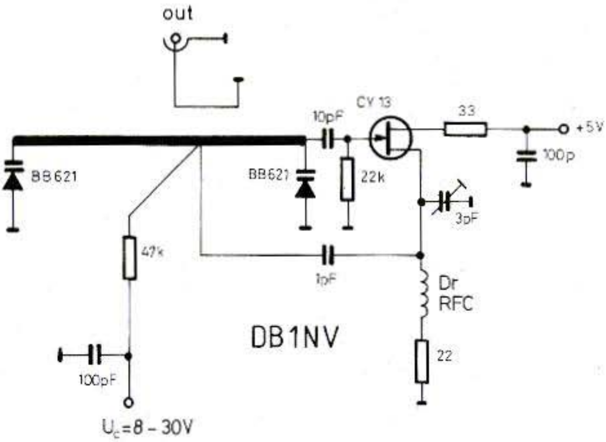

Fig. 6:
A 1 to 1.6 GHz GaAs-FET oscillator, Choke: 3 turns 0.3 CuL, 1.5 mm dia

- Oscillator refuses to oscillate:
  Load coupling too tight, feedback coupling incorrectly chosen, varicap diode wrongly connected or a transistor defective – the author has often found transistors which tested good under DC conditions but failed at the working frequency.
- Unstable frequency:
  Tuning voltage power supply poorly regulated.
- Sharp drop in output power at band ends:
  Optimize both the load coupling and the phase of the feedback.
- Output gaps in the tuning range with frequency jumping:
  Parasitic resonances in the circuit caused by long RF leads or unsuitable components for the frequency under consideration – the author thought he was being very good by using, for the 1 - 1.5 GHz oscillator, a 100 pF chip capacitor for the DC blocking to the transistor base because it was exactly the same width as the stripline. The result was a reverse tuning with a hysteresis point around 1.15 GHz – the self-resonant frequency of the chip capacitor. The problem was solved by replacing the chip capacitor with a simple disc capacitor.

6. CONCLUSION

With these few examples, relatively little outlay and using standard components from the television technology, tunable test oscillators may be made to cover the range 100 MHz to 2 GHz. Besides their application for the testing and alignment of antennas and filter networks, they can be used as the basis for a simple spectrum analyzer or a sweep generator.

Dieter Schwarzenau and Bernhard Kokot

Home - Constructed Frequency Counter Part 1

The measurement of frequency, for the radio amateur, is probably the most important measurement of all. In the days of the tube, the grid dip-meter or an absorption wavemeter indicated the frequency whereas nowadays it is possible, with little effort, to build a highly accurate digital frequency counter. There are construction articles in profusion which have been published.

The following description of a frequency counter with designation DL 0 HV was evolved with the object of building an inexpensive, small frequency counter which would possess a high resolution in the higher frequency regions. The inclusion of other special functions such as event counting, frequency ratios, time intervals was deliberately omitted.

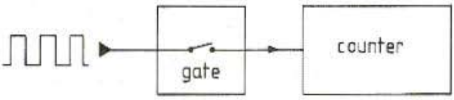

Fig. 1: Principle of a digital frequency measurement

1. PRINCIPLE

The word "frequency" is used in the connotation of periodically reoccurring events, e.g. electrical oscillations. It may be defined as the number of these events which occur in a stated interval of time. The simplest method of determining the frequency, is to count the number of the events occurring during a known time. The diagram of **fig. 1** shows that two functions are required, the counter and a gate, which, in the simplest case, consists of a switch.

Assuming that the counter is set to zero and the gate is opened for a period of one second, then the train of input pulses would be directed to the counter and for each pulse the counter would increase by 1 during this period. At the end of the open gate period the number of counted pulses can be given the unit "Hertz".

For the next measurement, the counter must be reset back to zero and the gate again opened for another second. In order that this process be continually repeated, the block diagram indicating this principle would have to look like **fig. 2**.

After every measurement cycle, the count is passed to a store which has the job of holding the

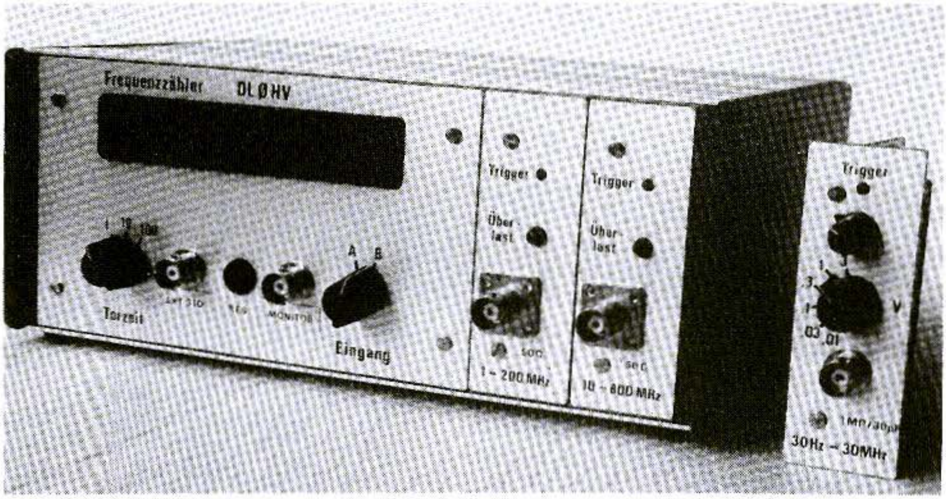

Photo A: The completed instrument together with plug-in unit

contents steady, both during the count and until sufficient time has elapsed for the indicator (read-out) to be read. The control unit resets the counter, closes the gate after a pre-determined time, clears the store and also re-enables it.

1.1. Accuracy and Resolution

For a gate time of one second the result may be read out, on the display, directly in Hertz.

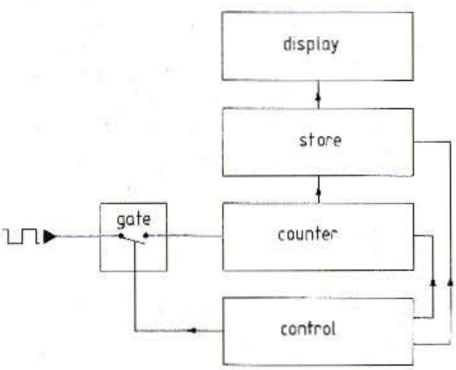

Fig. 2: Principle of a digital frequency counter

If the gate time is longer or shorter than its pre-selected period then the read-out will be inaccurate. A pre-requisite for the correct measurement is, therefore, that the gate period must be as exact as possible.

Another source of error arises because the counter recognizes the input pulses by either the rising flank or by the falling flank and counts accordingly. If the gate closes shortly before an input pulse has been completed, it may not be counted even though it is almost completely included in the given time frame **(fig.3)**. By the same token, an input pulse flank may occur shortly after the gate has opened. In this case, the counter indicates one pulse too many.

This unavoidable inaccuracy is known as digitalization error and in the case outlined above it amounts to ± 1. Its influence is dependent upon the frequency to be measured and the gate time chosen to effect the measurement. For example, if a frequency of two Hertz (2 Hz) were to be measured, using a gate period of one second, the outcome would be a read-out of 1 Hz, 2 Hz or 3 Hz, i.e. an error of 100 %. The gate time period must therefore be long enough to embrace as many input pulses as possible but this, of course,

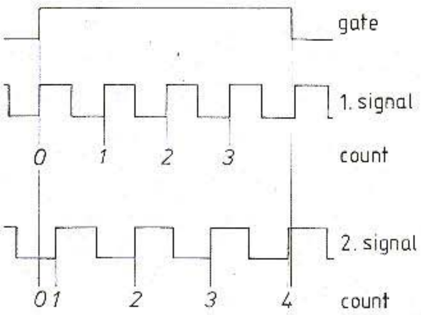

Fig. 3: Example showing how digitalization errors arise

entails a long wait for the indicated result. The input frequency under measurement may also, during this time, suffer sudden shifts which would not be registered. In practice, the usual gate periods used in a frequency counter are selectable in the range 0.1 to 10 seconds.

Another criterion for the quality of a frequency counter is its upper frequency limit. If it is lower than the frequency to be measured, then a digital pre-scaler can be employed to divide the frequency prior to its introduction to the counter. This has, however, the disadvantage of decreasing the resolution by the same factor as the scale-down. This means, for example, that if a frequency of 1 GHz is to be measured using a counter of only 10 MHz capability, a pre-scaling factor of 100 would be required. If the resolution required was 1 Hz, the gate time would have to be 100 seconds. If the basic counter had an upper frequency limit of 100 MHz then only a 10 second gate time would be required with a division of 10 in the scaler.

2. DESIGN PRINCIPLES

One of the guiding principles in the development of the DL 0 HV frequency counter was the demand for an upper frequency limit which was as high as possible.

Frequencies in the two metre band should be capable of being counted directly. This automatically precludes the use of TTL logic for the first counter stages. Instead, ECL logic elements were chosen with a frequency specification of 150 MHz. Constructional experience has since shown that many examples work up to 200 MHz. For still higher frequencies, the counter is provided with a pre-scaler. The scale-down factor should be as low as possible in order not to compromise the resolution unduly. As there are economical ECL pre-scalers on the market with a division factor of 4 the only thing to do was to prepare a suitable gate period to give a direct read-out.

Gate periods of 0.1, 1 and 10 seconds were chosen, which, with the provision of the pre-scaler, would have to be shortened by a factor of 2.5 automatically. This means that up to 150 MHz a resolution of 0.1 Hz is achieved, above that,one Hertz. The accuracy is always expressed at the highest frequency and is 6.6×10^{-10}. If this accuracy is to be realized then the accuracy of the time-base (gate) should not be any lower. The utmost possible accuracy has already been achieved with little effort.

The crystal oscillator, used for the time-base reference frequency, must be thermally stabilized and optimized for a long-term stability. The requirement for a suitable temperature-trimmed crystal is unavoidable.

The counter was housed in a small module container from the firm Bicc-Vero. It is compact and all modules have easy access. In juxtaposition to the counter unit there are provisions for two plug-in units, pre-amplfier or pre-scaler, which can be quickly changed as the need arises.

2.1. Modules

The frequency counter comprises the following six modules: –

1. Crystal oscillator
2. Counter control
3. Digital counter unit

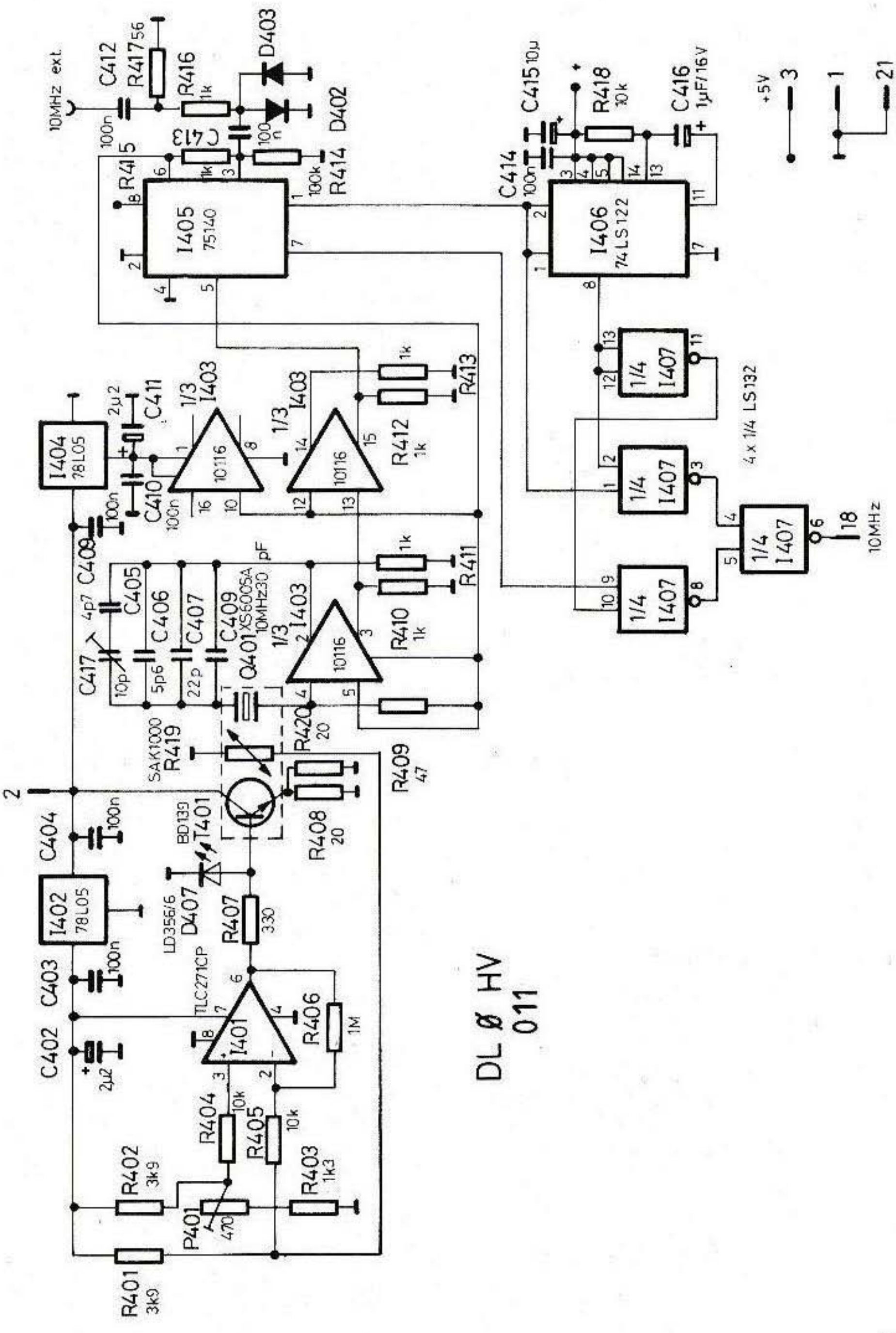

Fig. 4: Reference frequency oscillator circuit diagram

4. Display and operating unit
5. Pre-amplifier / pre-scaler
6. Power supply

Each of these six modules is constructed on its own dedicated printed circuit board. Modules 1 to 4 form the basic counter and are located behind a common front panel. The connections between them are made by open resistors and plug-in connectors.

At the moment there are three plug-in modules to chose from: –

1. A pre-amplifier 30 Hz - 30 MHz, 1 Ω/30 pF
   Sensitivity: 2 mV; 100 V max. input
2. A pre-amplifier 1 MHz - 200 MHz, 50 Ω
   Sensitivity: 10 mV, 5 V max. input
3. A pre-amplifier with a pre-scaler
   50 MHz - 800 MHz, 50 Ω
   Sensitivity: 5 mV, 5 V max. input

The housing offers the possibility to fit two of these plug-ins. A selector switch on the front panel allows the desired signal from the plug-in to be connected to the basic counter unit. The transmission of the input signals is carried out, at ECL level, by cables routed via the back wall of the housing. The power supply unit is built in a box specially provided and mounted behind the back wall wiring.

2.1.1. The Crystal Oscillator

The circuit diagram of the crystal oscillator is reproduced in **fig. 4**. The active element used for the oscillator itself is the ÉCL power driver MC 10116 (I 403). The crystal is driven in series resonance and its frequency may be finely trimmed using capacitors C 405 to C 408. A further power driver is used as a buffer amplifier and the third portion of this chip remains unused.

The enclosure bounded by the dotted lines and containing components T 401, R 419 and Q 401, indicates that these elements should all be mounted in close thermal contact with each other. The circuit of I 401 is a temperature control for the crystal oven heater. The heater element is a transistor T 401 which is controlled by a bridge circuit balanced by a temperature sensor R 419 with resistors R 401 to R 403. Potentiometer P 401 is used to adjust to the required temperature. The LED, D 401 indicates the regulation condition and may be mounted on the front panel. It is extinguished when the required temperature has been achieved.

Both the oscillator and the regulation circuit possess their own voltage stabilizing circuits I 401 and I 404. As the gate timing control must be supplied at TTL, a level change is necessary. This is carried out by the SN 75140 (I 405). This IC contains two power receptors each with two differential inputs and a TTL output. One power receptor is fed by the oscillator signal and the other serves as an input for an HF reference signal. A minimum input amplitude of 100 mV is required for this input signal. The reference signal is limited by diodes D 402 and D 403. The other two inputs of the differential pair are connected to the reference voltage output of the ECL IC. The voltage at this output lies exactly between the two possible ECL levels. In order to save a change-over switch between internal and external reference oscillators, the external reference coming via I 405 is fed to a retriggerable monoflop which effects the change-over automatically via I 407 when an external reference is connected.

The supply to the oscillator module is a stabilized 5 V and an unstabilized 12 V (approx.) for the heating and the two on-board voltage regulators.

2.1.2. The Counter Control

The counter control pulses are derived from the basic counter 10 MHz reference frequency oscillator by means of this unit (**fig. 5**). These pulses control the counter gate times, the delivery of display contents and the counter reset.

The simplest way to derive the gate-time period is to divide the 10 MHz reference frequency down

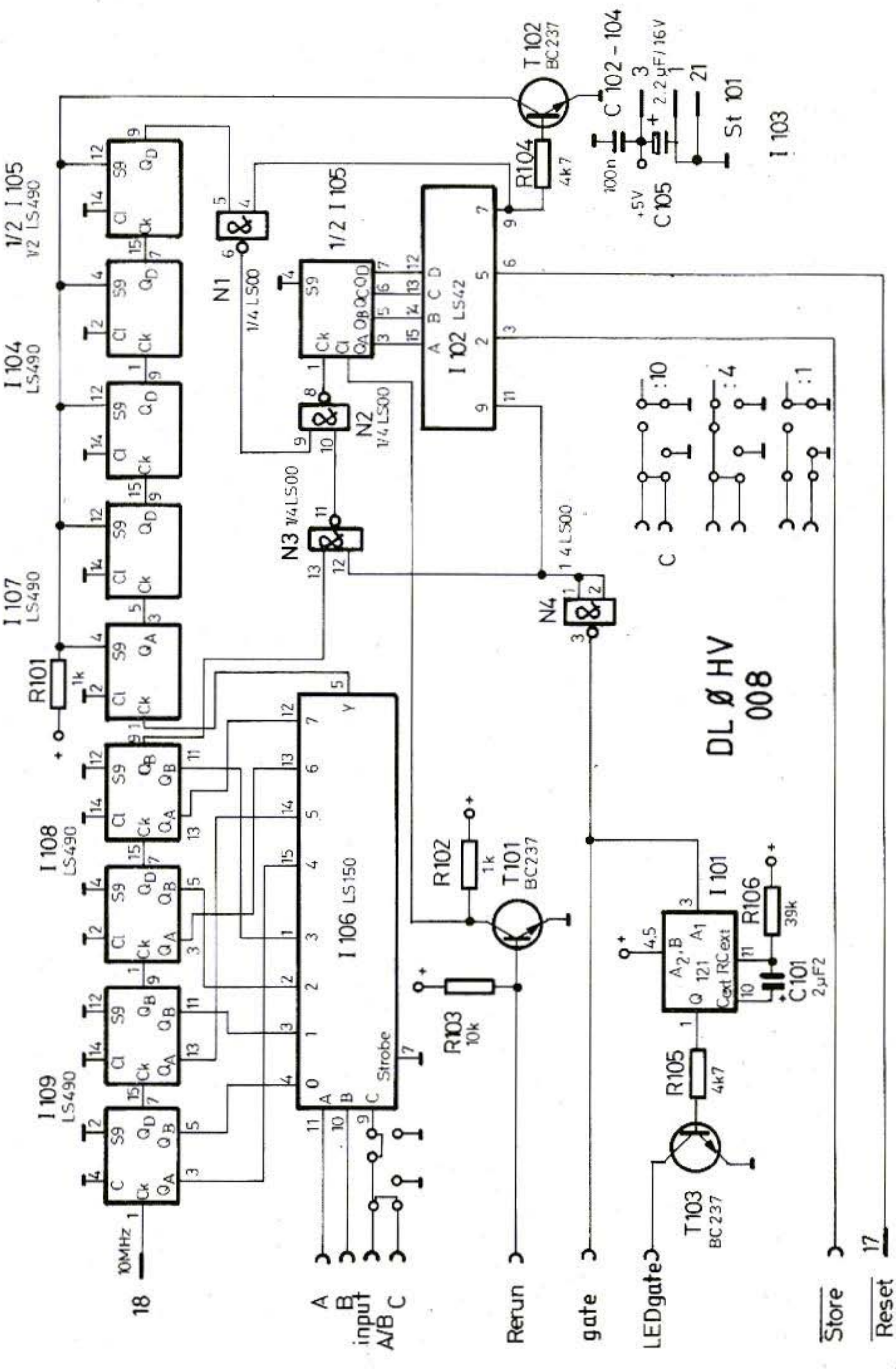

Fig. 5: Counter control schematic

until the desired gate period is achieved and use that to drive the gate directly. That would mean that the interval following every count cycle would be as long as the count itself. For example, a selected gate period of 10 seconds would entail a wait of 20 seconds before the result is displayed. In order that this situation is avoided, the counter control is so arranged that the counting pause is independent of the selected gate period and lasts only 7 ms. This concept requires careful attention to the differing gate duration times at various signal paths as the measurement accuracy depends upon an exact adherence to the gate pulse period.

As in the case of the direct division concept, a divider chain is required, but in this case comprises two paths. The first path consists of I 109 and I 108. Every second output of the decade divider is lead to the input of I 106, an 8 to 1 multiplexer. Depending upon the level at inputs A, B and C, one of the 8 inputs are connected to the output Y. Altogether eight frequencies corresponding to eight gate periods can be selected.

The second part of the divider chain consists of five further decade counters which may be all set to "9" via input S 9.The period of the signal at the end of this divider chain is that of the selected gate period. It is fed via two NAND gates to a further decade counter which controls the sequence of operations. It is connected to a BCD-to-decimal decoder (I 102) in order that for every counter display a dedicated output circuit is available. Output 9 operates the gate. As the outputs of the decoders are all "low" when activated, an inverter (N 4) is necessary. A monoflop, also driven at the same time as the gate, causes an LED to extinguish every time the gate closes.

During the counting phase the control counter is in condition "9" and the output 9 of the decoder is "low". The next falling edge of the pulse delivered from the divider chain is fed to the clock input of the control counter and sets it to zero. This shifts the decoder output 9 to "high" and closes the gate via N 4. At the same time, the gate formed by N 3 opens and it passes 1 kHz pulses from the first part of divider chain N 2 to the clock input of the control counter. This starts counting in quick succession. At the counter condition of "2", the transition line "STORE" is set to "low" and the frequency to be displayed is passed into the display memory. The output 5 of the decoder operates the "RESET" line of the frequency counter. When the control counter reaches condition "7", all the divider counters in the second half of the divider chain are reset to "9" via transistor T 102. Simultaneously, the input of gate N 1 is pulsed in order that its output remains on "high". By this means, the next 1 kHz impulse may be fed via N 2 and N 3 to the control counter input driving the counter up to "8". The output of N 1 returns to "low" and N 2 blocks the rest of the 1 kHz pulse train. As the S 9 inputs are now again free the counters of the second divider chain are set to zero by the next trailing edge of the multiplexer signal. This negative-going flank is also fed via N 1 and N 2 to the input of the control counter which again receives the condition "9" and via its decoder output opens the gate. First before the gate is opened, the divider chain is in the same condition as it was shortly before the gate was closed. The pulse flanks which switch the gate have identical periods.

The counter cycle can be interrupted, at any time, by means of the input "RERUN". The control counter is set to zero via transistor T 101 and thereby priming the circuit for a new counting cycle. This option is useful for counts using long gate periods.

The eight possible gate periods are divided into two groups of four. The choice of any of the four gate periods is effected via the inputs A and B of the multiplexer. Their lengths are 0.01 s, 0.1 s, 1 s or 10 s, also 0.004 s, 0.04 s, 0.4 s or 4 s.The first four of these gate periods are for use with decade pre-scalers and also direct inputs to the basic counter. The other gate periods allow the use of the economical ÷ 4 pre-scalers. The selection of the sets is effected via input C of the multiplexer which is switched either to ground or onto the control line DIVIDER by jumper pins. The second jumper serves to select the decimal point logic control and connects line C with line "input A/B" when a pre-scaler has been fitted into input B. Otherwise "C" is directly connected to ground.

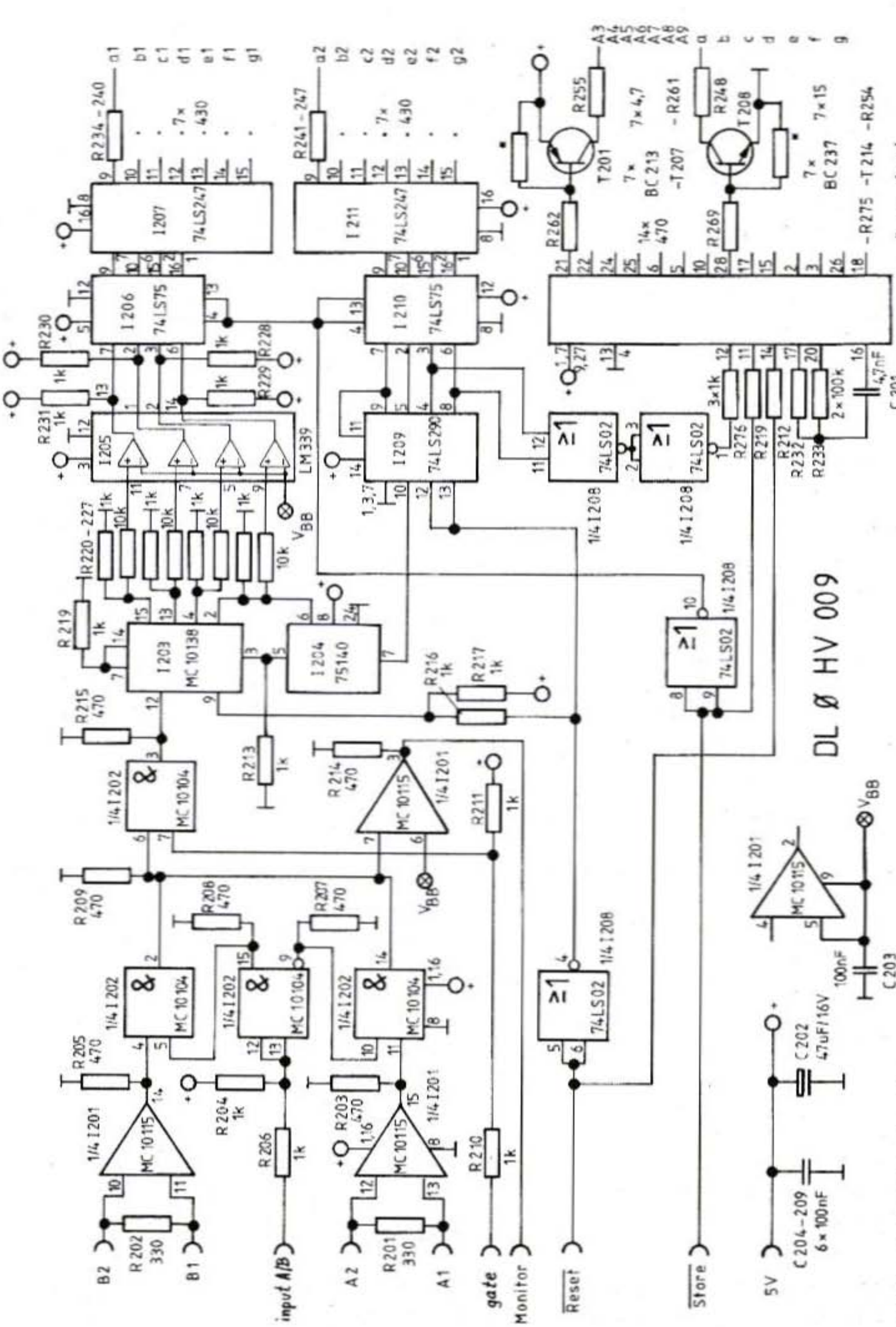

Fig. 6: Counter unit schematic

2.1.3. The Digital Counter Unit

The counter unit **fig. 6** has two symmetrical ECL inputs to which the pre-amplifiers or pre-selectors may be connected. Owing to the employment of a special line receiver (I 201) and the 330 Ω termination resistance an interference-free operation is assured even at high frequencies.

The gate is connected to either of the two inputs by means of "input A/B". The selection and control is effected by three AND/NAND gates (I 202). As ECL outputs represent an open emitter, they may be connected together without any trouble. The fourth NAND gate serves as the gate. the line receiver at the gate input is used as a monitor output buffer stage. The signal to be counted may be observed at this point by means of an oscilloscope. This facility is particularly useful when distorted input test signals are to be measured which give different counts according to the position of the trigger level.

Behind the gate lies the first counter stage I 203. This is a BCD counter, using ECL, which can work from zero up to a frequency of 150 MHz. Matching the ECL level to the TTL indicator store (I 206) is accomplished by connecting all four BCD outputs with a comparator. The necessary reference voltage is available at the pin of the line receiver. The coupling resistor of 10 kΩ avoids loading the outputs too much during the counting process. With I 207, a BCD-to-seven-segment decoder, the contents of the indicator store may be seen via the lowest position of the read-out.

The second counter stage uses TTL logic and thus requires a level change. A comparator cannot be used here because the conversion process must operate at a frequency of over 15 MHz (due to the asymmetrical duty cycle). Therefore, a special line receiver (I 204) for symmetrical transfer, has been used. As the ECL counter module also has its D output inverted, both inputs may be connected directly.

The TTL counter stage uses a simple BCD counter which drives the indicator store with a seven segment decoder (I 210, I 211) in exactly the same way as the ECL stage.

The following counter stages use an LSI (I 212) which, besides having seven BCD counters, contain all the necessary indicator stores, a multiplexer and display drivers. The drivers, using only 5 V, are not in the position to compete with the statically driven seven-segment decoders and therefore, all multiplex outputs are fitted with external driver transistors (T 201 to T 214).

The limiting frequency of this integrated counter circuit is about 6 MHz for a 5 V supply voltage.

With a signal frequency to be counted of 150 MHz, the TTL counter stage delivers an output signal at a frequency of 1.5 MHz. This output signal has, however, a 1 to 4 duty cycle as the period belongs to a frequency which lies higher by a factor of 2.5. Although this frequency is well under the specified limits, in practice difficulties were encountered. The duty cycle was therefore converted to 1 by means of two NOR gates used as an OR gate and a second output of the TTL counter.

The control of the unit count is made via the inputs "gate", "$\overline{\text{RESET}}$" and "$\overline{\text{STORE}}$". When the "store" line is low, the display store accepts the contents of the counter stages. When the "$\overline{\text{RESET}}$" is activated, all counter stages are reset to zero. As the TTL circuits and the ECL counter require opposite polarity signals, two gates of I 208 are used as inverters. The level change TTL to ECL is made by the two 1 kΩ resistors. One lies in the connecting line and the other serves on the ECL side as a pull-up resistor.

2.1.4. Display and Operating Unit

Besides the display and operating portions, this module also contains the logic for the decimal point control (**fig. 7**). In order to simplify this, every third decimal position from the 1 Hz display, is

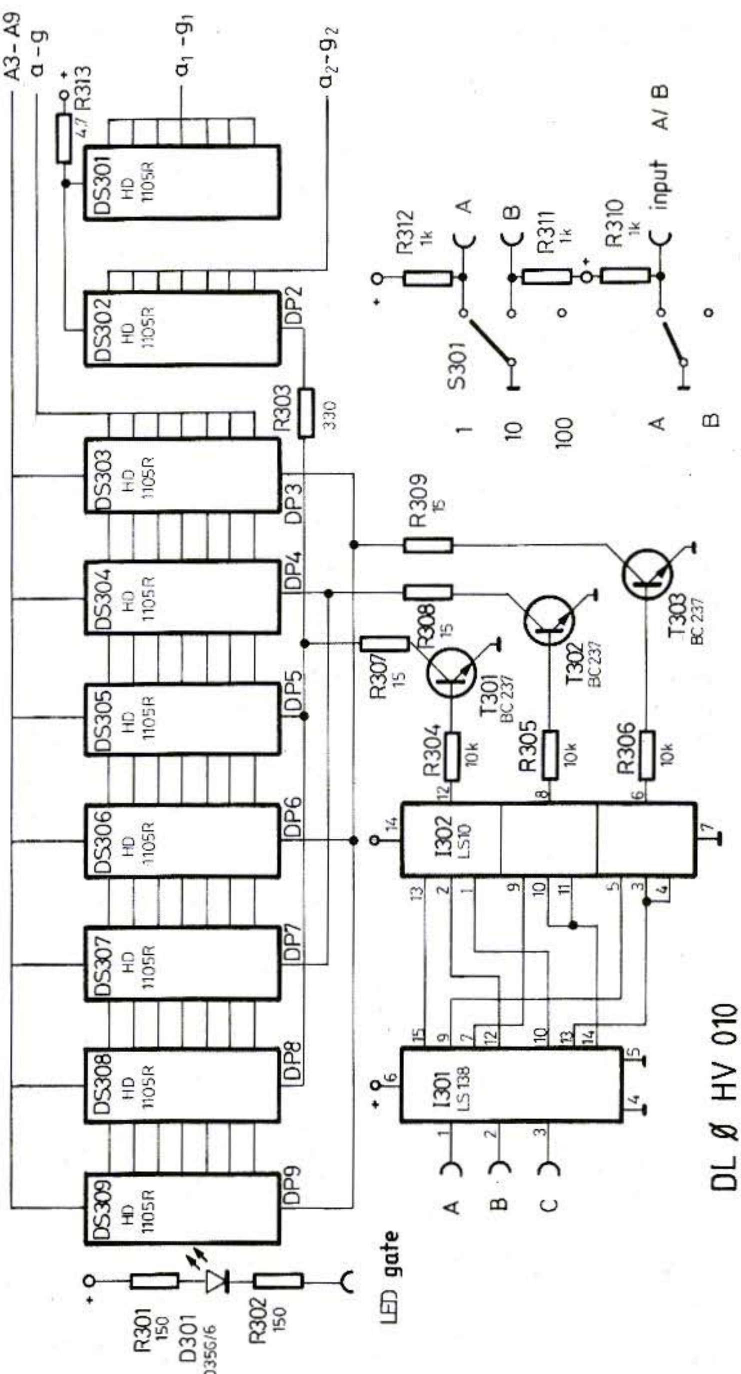

Fig. 7: Display and operating unit schematic

controlled. This means a maximum of three decimal point positions, in a nine indicator display, all on at the same time and representing 1 kHz, 1 MHz and 1 GHz. There are then three groups of decimal points one of which must always be on.

The control is effected by three transistors (T 301 to T 303). These, again, are addressed by three AND gates (I 302) whose inputs are connected to a 3 to 8 binary decoder (I 301). The level at inputs A and B of this binary decoder contain the information concerning the selected counter gate time. Input C is normally low and is only addressed when the input unit in use has a division factor of 10. In this case, the decimal point is shifted one position to the right.

Another LED (D 301) also forms part of the seven-segment numerical display inasmuch, that during the process of counting it illuminates during the gate period. By means of this diode, the start of a counting period may be recognized when a long count duration is being employed.

Two rotary switches form the service controls: one is a three-position switch and selects the gate period, the other gate period 0.01 s or 0.004 s, supplied by the counter control, being unused. The other switch determines which of the two plug-ins will be connected to the counter.

2.1.5. The Counter Input Plug-in Units

It was mentioned in the introduction that the quality of a counter is dependent upon the accuracy of the time base and the resolution offered by the counter. In the HF measurement area, the characteristics of the input conditioning circuit must also be considered. They are there to match the signal to be measured to the required logic level of the digital counter. In order to obtain as much versatility as possible, the following demands are placed upon this unit: –

1. A large as possible pass band
2. A high sensitivity (in the order of a few mV)
3. Overload-withstanding inputs (at least 0.5 W)
4. Either a constant 50 Ω input impedance or a high impedance with very low capacitance

2.1.5.1. High Impedance Input Unit

In many cases it is desirable that the item-under-test should be as lightly loaded as possible by the test instrument. Accordingly, an input unit was developed which has an input impedance comprising 1 MΩ at 30 pF (**fig.8**). It has six selectable voltage ranges. The parallel switched capacitors C 601 to 603 prevent that the division ratios are not rendered frequency dependent by parasitic capacitances across the divider chain resistors R 601 to R 603 and the wiring etc. The signal-under-test is lead to an N FET via a protection resistor R 604. This FET is connected as a source follower. The two anti-parallel connected diodes D 601 and D 602 limit the gate voltage during over-voltage conditions. If capacitors C 601 to C 604 are sufficiently voltage-rated, even application of the mains voltage will not cause damage.

The capacitor C 606 acts as a compensation capacitor and prevents the fall-off in amplified voltage with frequency via the drain gate capacitance. The source resistance is formed into a further voltage divider chain. Together with the input divider, a six-range division is accomplished.

As source followers have a relatively high output resistance, a further impedance converter T 602 is employed. Immediately following the coupling capacitors C 607 and C 608, there is a simple low-pass filter having a cut-off frequency of 16 MHz. The limitation of the frequency response is necessary as the high-impedance input circuit is very susceptible to interference. Owing to the use of ECL circuit drivers as amplifiers,

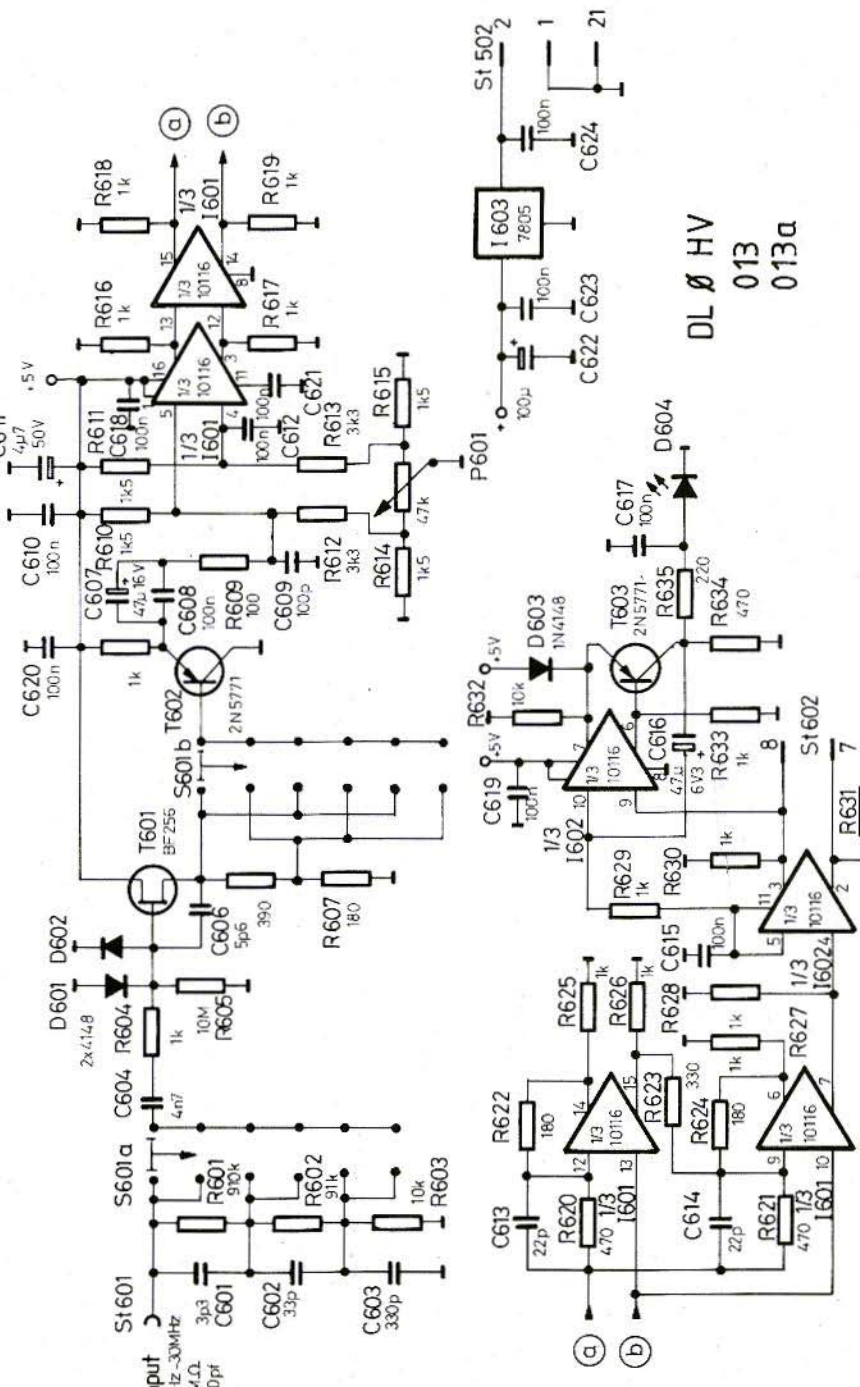

Fig. 8: High-impedance plug-in schematic

there is a very large pass band achieved together with a high total amplification factor.

The DC level for the ECL drivers is produced via R 610 to R 615. Potentiometer P 601 provides a limited adjustment to the input trigger level. This control becomes important when measuring highly distorted signals.

Following two simple amplification stages, giving some 20 dB, are drivers which are coupled by resistors. Capacitors C 613 and C 614 result in a hysteresis which serves to mitigate the effects of noise on the measurement.

Of the two final ECL drivers, one is for the gate and the other is used as a multivibrator. The multivibrator controls an LED which is useful to assess the trigger adjustment. If it is too low, the LED remains unlit and when it is too high it stays on continuously. If, however, there are input pulses, the LED starts to blink. Frequency-determining elements are C 616 and R 629.

This plug-in unit is suitable for frequencies in the range 20 Hz to 30 MHz and exhibits a sensitivity under 15 MHz of 2 to 6 mV. The influence of the low-pass filter becomes more evident at higher frequencies (**fig.9**), without it, the sensitivity does not drop drastically until about 100 MHz.

2.1.5.2. 50 Ω Plug-in Unit for 1 - 200 MHz

It is not really meaningful to make a high-impedance input amplifier for frequencies above 30 MHz. With this module (**fig. 10**), it is possible to work with frequencies from about 1 MHz to the limiting frequency of the first counter stage. The input stage is protected from overload voltages by a self-regulating PIN diode attenuator which works without an external controlling voltage. This lies in parallel with a rectifier circuit which controls a comparator with the rectified DC, the purpose of which, is to provide an LED overload indicator. The trigger level is adjusted by preset P 701. Both comparator inputs are symmetrically wired in order that the adjustments are not effected by temperature.

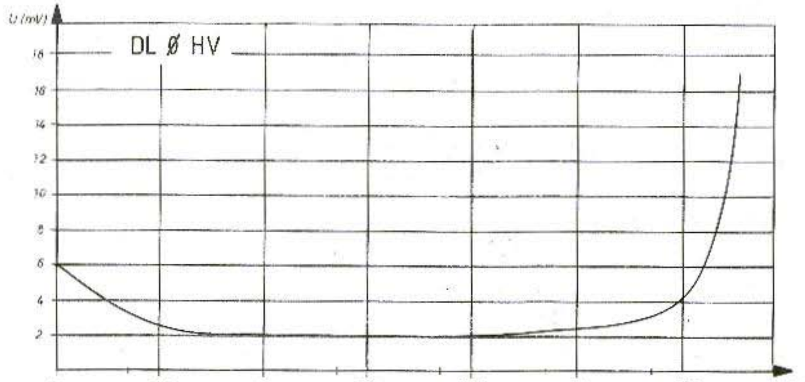

Fig. 9: Sensitivity characteristics of high-impedance plug-in

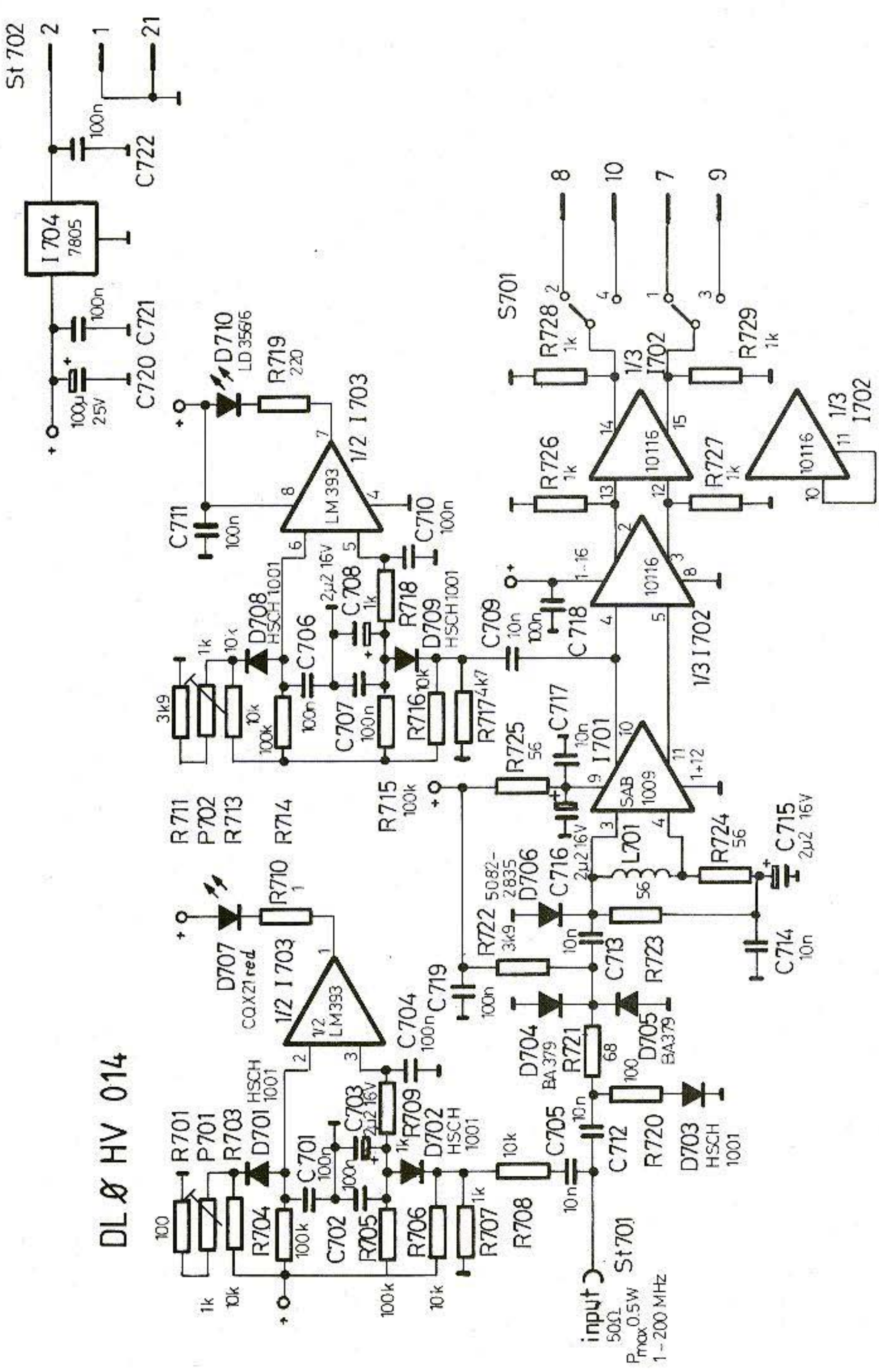

Fig. 10: 50 Ω pre-amplifier plug-in schematic

An ECL limiting amplifier (I 701) follows the PIN diode attenuator. Inductor L 701 serves as matching for the module's balanced input.

The output is delivered by two ECL line drivers, the third one (I 702) in the chip being unused.

Between the first and second amplifier stages is placed a further rectifier stage which is constructed in exactly the same manner as the first one. The accompanying comparator lights an LED (D 710), when a signal, whose amplitude is sufficient to trigger the digital section, is present at the input. The trigger level is controlled by preset P 702.

This pre-amplifier plug-in exhibits a sensitivity of less than 20 mV (**fig. 11**). Through the PIN diode it is capableof withstanding an input of 0.5 W. A still greater input would result in the destruction of R 721. Experience has shown that other components do not share the same fate. This is also the case when the unit supply voltage is not switched on. In order to ensure that this protection is maintained, it is as well to keep the input frequency, at all times, to above 1 MHz as the PIN diode alters its characteristics below this frequency.

2.1.5.3. 50 Ω Plug-in Unit for 50 - 800 MHz

In order to be able to measure the frequency of signals above that of the basic counter unit, the 50 Ω plug-in was modified in order to include a pre-scaler (**fig.12**). As already mentioned, the higher resolution is obtained with the lowest dividing factor necessary for the input frequency to be measured. The division factor used in this scaler is 4 and uses a low-cost IC (about DM 12.-). As the gate-period control has already been prepared for this division factor, no further calculation is necessary to obtain the correct result – the display reads directly.

Apart from the transformer Tr 801, the circuit both in front of the pre-scaler and behind it, is identical with the previously described straight 50 Ω pre-amplifier plug-in. Tr 801 serves as an unbalanced

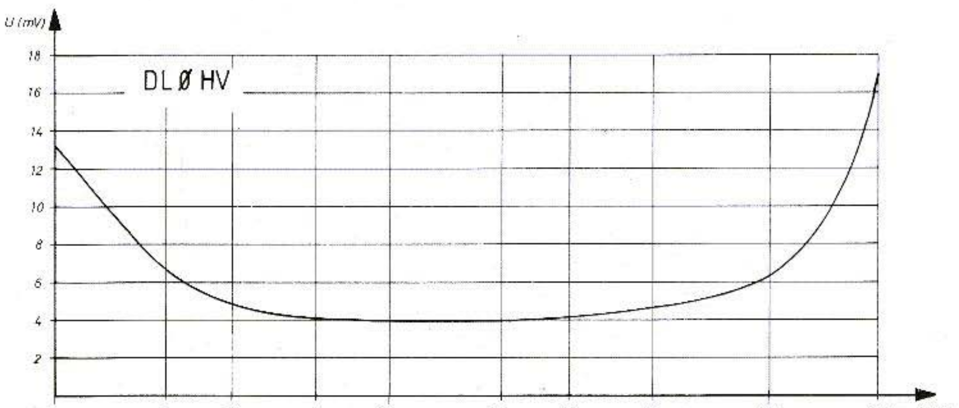

Fig. 11: Sensitivity characteristics of 50 Ω plug-in

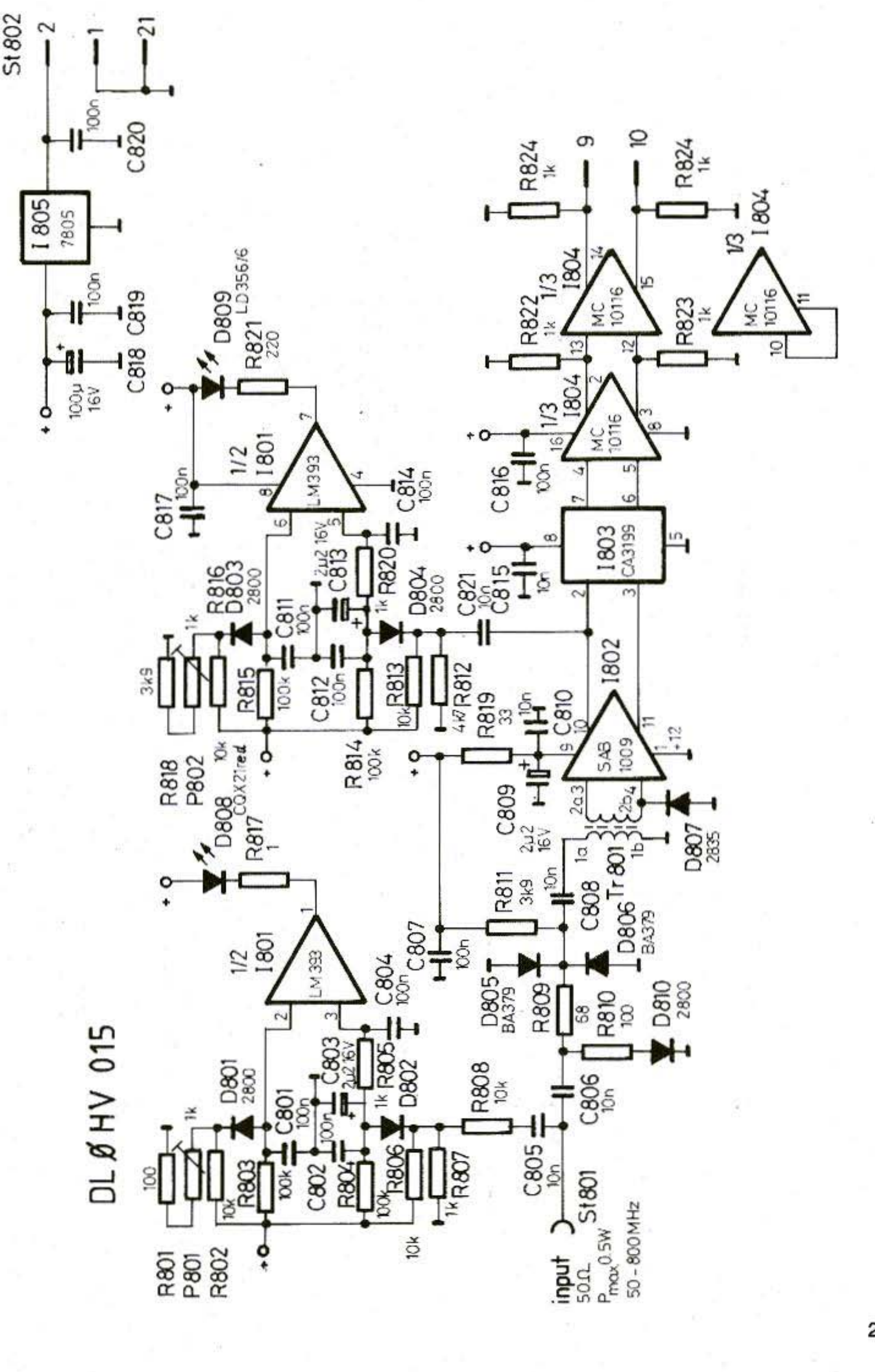

Fig. 12: Pre-amplifier with pre-scaler schematic

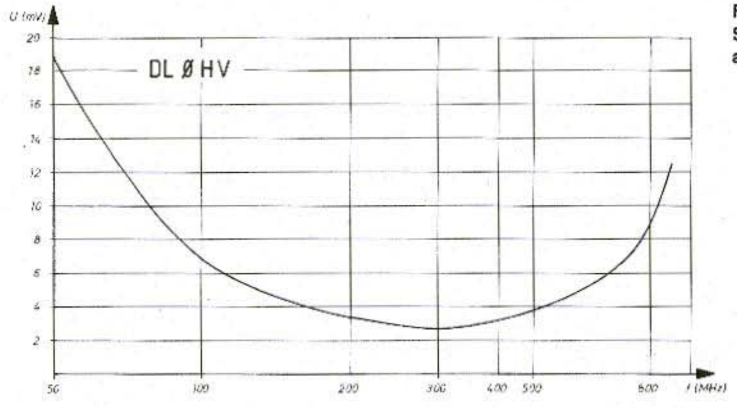

Fig. 13: Sensitivity of pre-amplifier with pre-scaler

to balanced transformer to match the input of amplifier I 802. The original circuit used a coil but this resulted in an unbalance and thereby to losses and hence lower sensitivity. The circuit using the transformer, however, has a maximum sensitivity of 3 mV at 300 MHz (**fig. 13**). Nevertheless, it is difficult to fabricate an extremely wideband transformer and the frequency range is thereby limited to a lower boundary of 50 MHz. Measurements down to 1 MHz, however,are still possible albeit at a greatly reduced sensitivity. Under that frequency, there is the problem of the efficacy of the PIN diode protection circuit being compromised.

2.1.6. The Power Supply Unit

Two power supplies are necessary for the whole counter including plug-ins: 5 V stabilized and 12 V unstabilized. The unstabilized voltage is used for the crystal oscillator and the plug-in units as they are both fitted with on-board regulators. The 5 V stabilized supply is used for the digital counter section. The unit must supply some 15 W of power.

In order that the counter may be supplied by an external battery, the stabilized voltage is obtained directly from the unstabilized supply. Otherwise, the power supply circuit (**fig. 14**) is

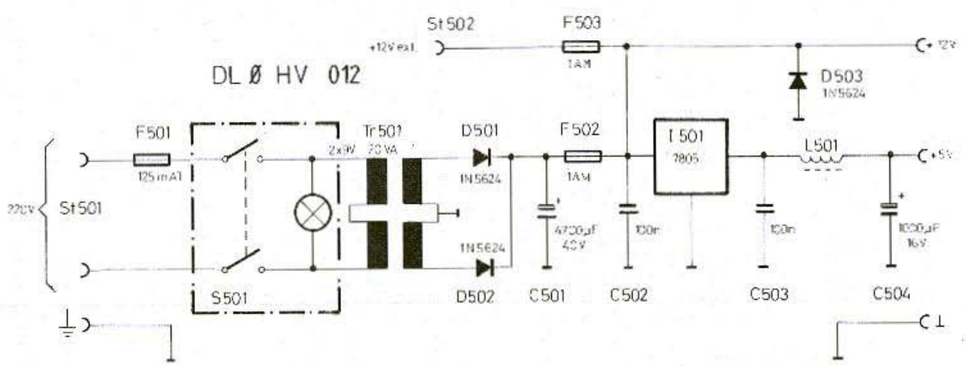

Fig. 14: Power supply schematic

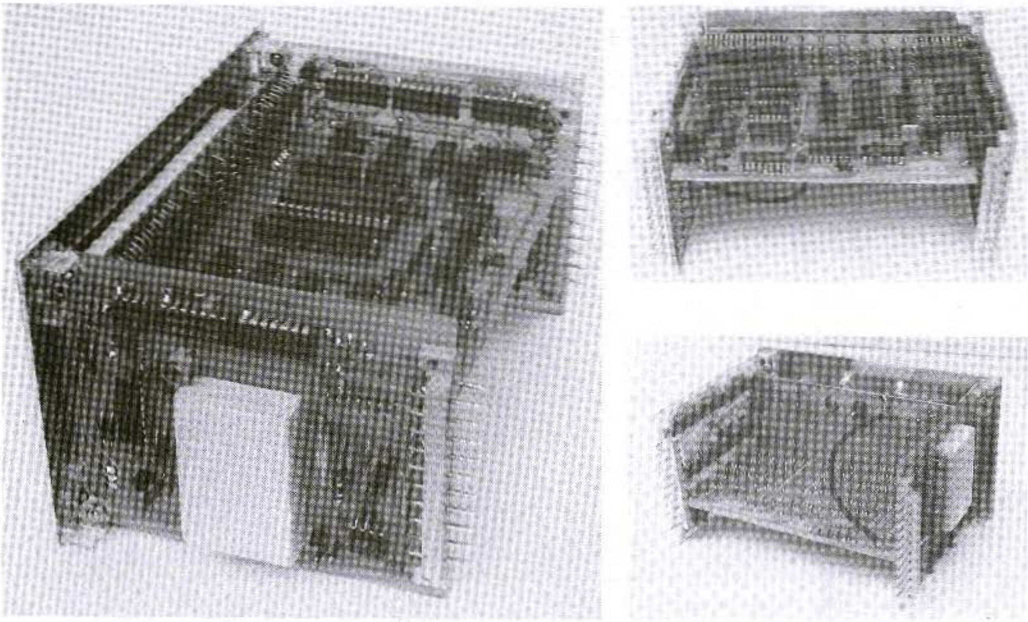

Photo B: Basic unit showing the thermostat in the foreground

quite straight-forward. The voltage regulators use a simple three-pin IC which must, on account of the high heat loss, be well cooled.

2.2. Construction

Through the use of a sub-rack system to house the equipment, all modules and cards are readily accessible and the plug-ins, pre-amplifiers or prescalers can be changed at any time. The latter point is particularly emphasized as only two plug-ins can be fitted into the basic unit but there is a choice of three. It should not be forgotten that the choice of such an equipment enclosure has also certain disadvantages. The large basic unit together with the wide digital display does not lend itself readily for splitting into modules each with a front panel. Also, a stable reference oscillator should actually have a secure, screened enclosure.

2.2.1. Basic Unit Construction

The basic unit lies behind a front panel and takes some 5/7 th of the available cabinet width. The oscillator and the control unit are fixed right and left as normal plug-in cards. The counter unit and the display and service card are fixed by the plug-in connector between them.

The display unit (**fig. 15**) and the counter unit (**fig. 16**) should be constructed first. The circuit for the decimal point control should not be forgotten on the counter card. The position of the components departs a little from that shown in the circuit diagram. Because the printed circuit boards are double-sided, but without being through-connected, it is more convenient and appropriate to solder in the ICs directly. Only the LSI chips should be fitted into IC holders. The resistor arrays are not symmetrical and care must be taken to get them the right way round – there's a

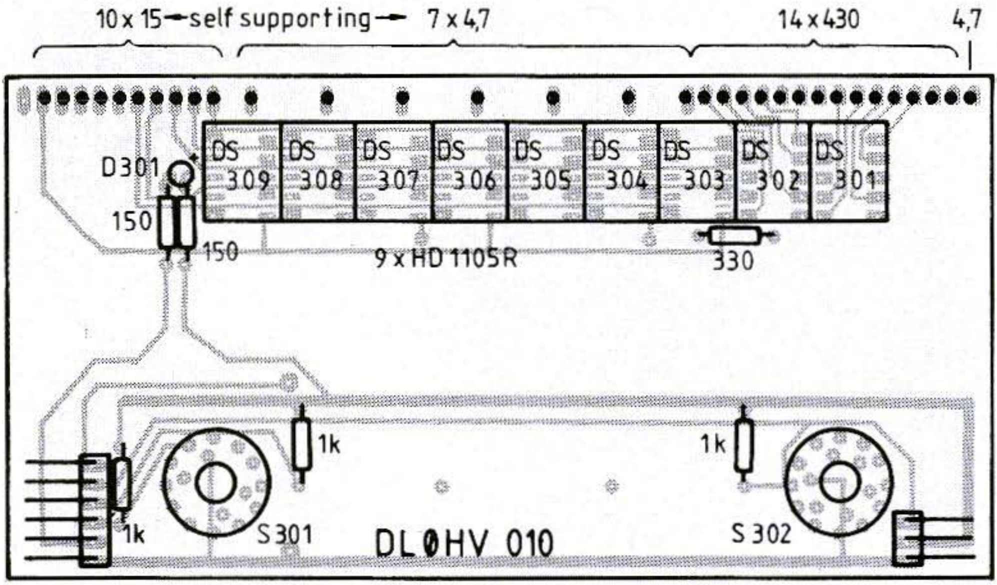

Fig. 15: Display board component plan

spot on the housing to mark the common lead. I 202 also, is fitted the opposite way around to all the other chips!

A holder for the display characters was used which may be soldered without difficulties, from above. The gap between the front panel and the display card is such that the display characters, fitted to the display holders, fit flush with the rear surface of the front panel. The rotary switch spindles should be cut to a length of some 12 mm before mounting them on to the front panel.

The display segment LED limiting resistors are wired freely suspended between the two cards and serve as a contact interface for them. They should just be mounted and soldered into the holes provided, in-line on the two boards, for them. The length of the wire-ends, between resistor body and PCB surface, should be about 8 mm (each side). Make all the connections to the counter card first and then, with the aid of a PCB holder or third hand, solder the ends into the display card. Then turn the two boards and at the same time the resistor connecting leads, until they are at right-angles with each other.

The BNC panel sockets, reset switch and the two control potentiometers are then fitted to appropriate holes in the front panel (**fig. 17**).

Next, the counter control and crystal oscillator PCBs are loaded with components according to the layout plans of **figs. 18 and 19**. Again, the ICs are directly soldered on to the boards.

The counter control cards connector covers some of the tracks on the top side of the board which cannot be through-contacted if the connector has already been fitted. Should through-contacts not

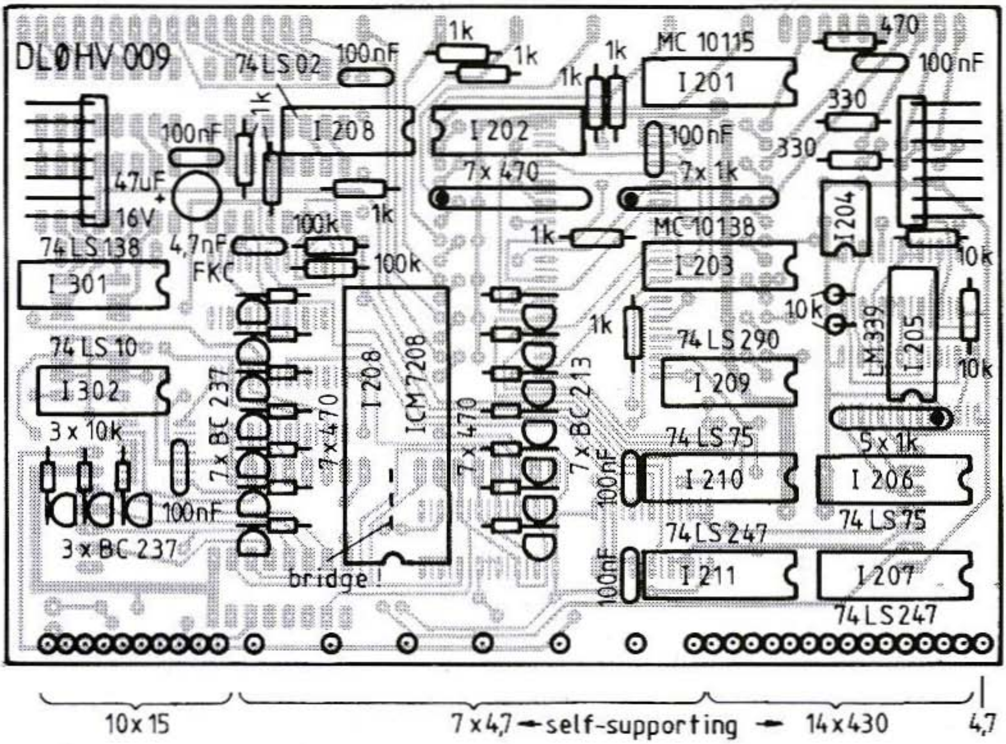

Fig. 16: Counter board component plan

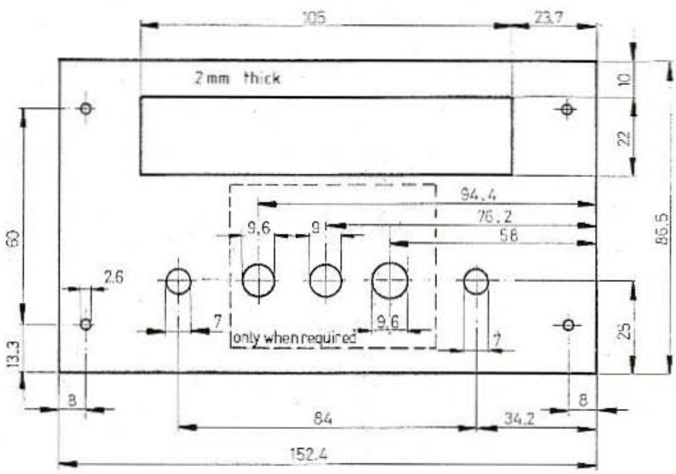

Fig. 17: Basic unit front panel dimensions

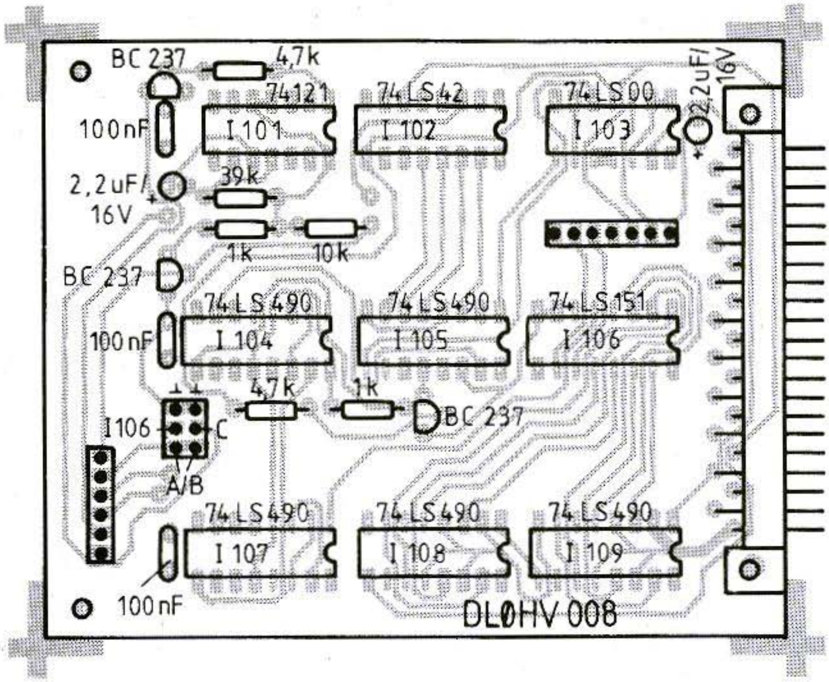

Fig. 18: Counter control component plan

be available, thin copper wire may be used. The wire is soldered to the top track, then lead through the board into the component connector and soldered on the underside.

The connector on the oscillator board must be fitted to the track side and soldered to the component side of the card. The crystal, the heater transistor and the temperature sensor should be mounted in very close contact with one-another. This is achieved by means of an aluminium strip 12 x 24 x 2 mm which is fixed to the transistor with an M 3 x 12 mm screw. The crystal and the sensor are simply adhered to this strip using two-component glue. The length of screw allows it to be secured through a hole in the PCB. In order to ensure that the heat is uniformly distributed along the strip, a suitable piece of expended polystyrene should be fabricated which is wrapped around the aluminium strip assembly together with the neighbouring two capacitors.

The two leading edges of these boards are then fitted with a piece of right-angle plastic strip which will support the boards when screwed on to the front panel. The oscillator is fitted to the right of the counter/display board and the control board to the left. After tightening all the screws, securing the plastic angle strip and front panel, all the boards are held tightly together. The BNC panel connectors and reset button can now be connected. The display cut-out in the front panel is

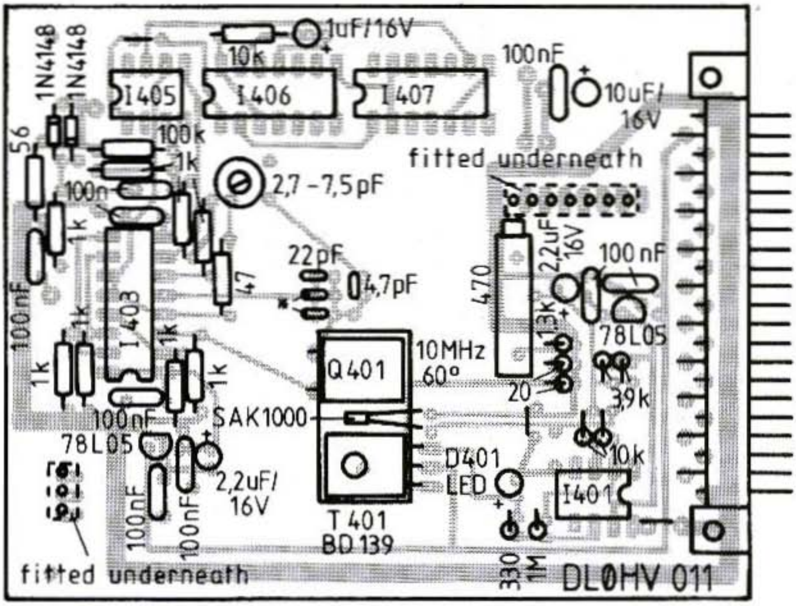

Fig. 19: Oscillator board component plan

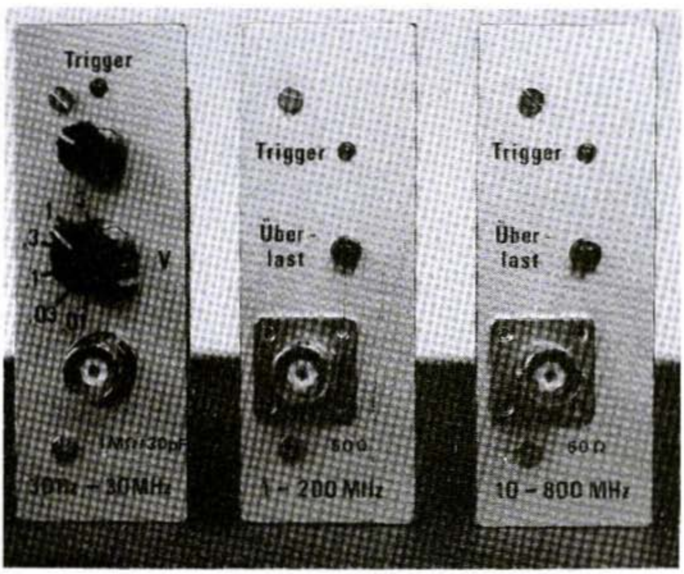

Photo C:
Three plug-in units

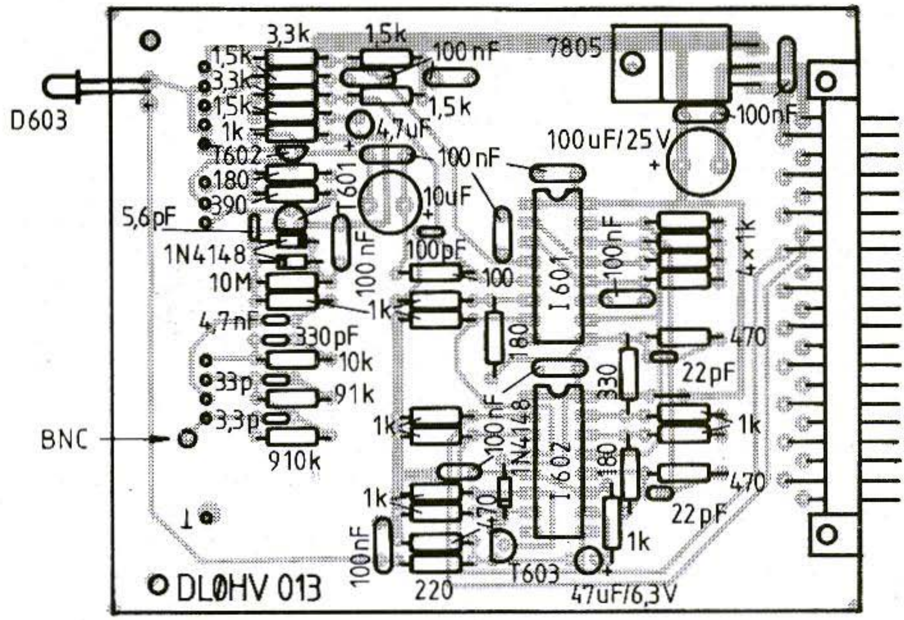

Fig. 20: High-impedance plug-in main board component plan

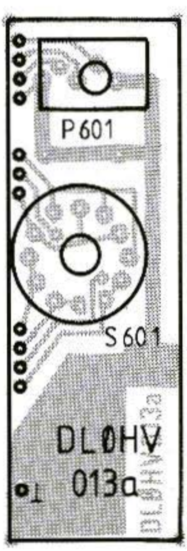

Fig. 21: High-impedance plug-in PCB component plan

fitted with a suitable piece of red acrylglass and secured with glue by its edges. Finally the knobs for the potentiometer are fitted.

2.2.2. High-Impedance Plug-in Construction

The high-impedance plug-in is constructed using two circuit boards (**figs. 20 and 21**). The smaller of the two is fitted in parallel to the plane of the front panel (**fig. 22**) and serves as the mounting for the rotary switch and the potentiometer. It is connected via twelve small wires with the main board. The shafts of the two control elements must be sawn off to a length of 15 mm before fitting to the unit.

When mounting the resistors for the first voltage divider chain, about 1 mm clearance should be given between the resistor body and the surface

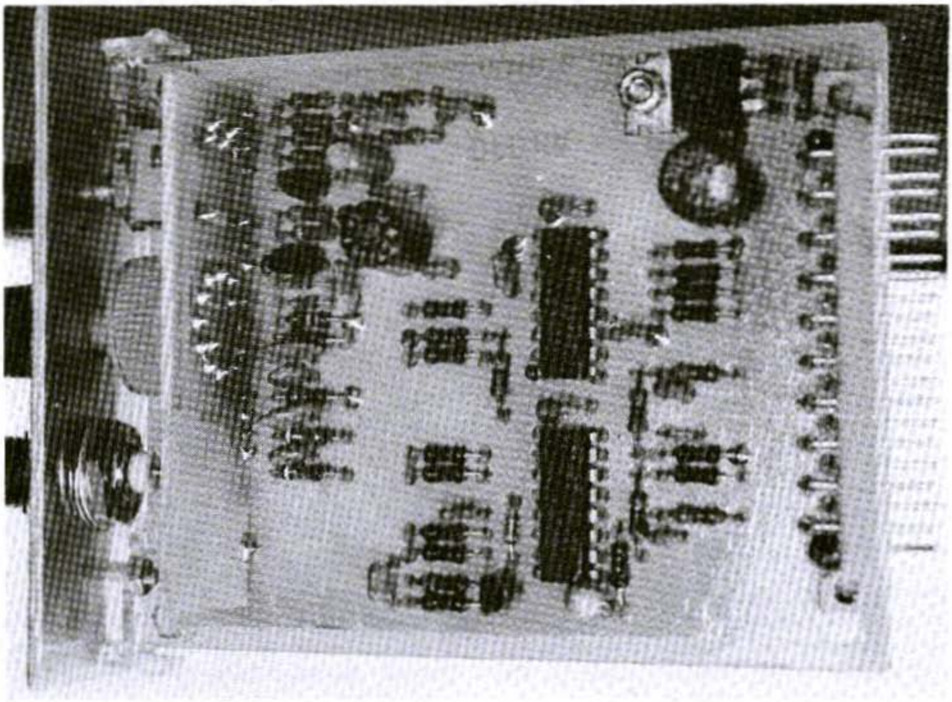

Photo D: High-impedance plug-in

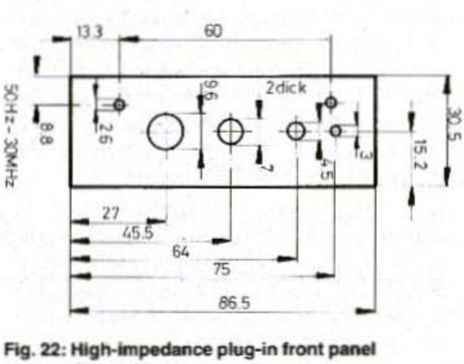

Fig. 22: High-impedance plug-in front panel dimensions

of the PCB. This precaution is to lessen the risk of voltage breakdown accuring during high-voltage inputs. For the same reason, the parallel connected capacitors should have an high as practical voltage rating. The voltage regulator can be screwed directly on to the printed circuit board. As the front panel is only fixed with plastic angle stock, an earth connection must be fabricated. This is the best provided by a soldering tag sweated to the top surface of the PCB and which is directly connected to the body tag of the front panel BNC connector.

Second, concluding part in the next edition.

Jochen Jirmann, DB 1 NV and Friedrich Krug, DJ 3 RV

Microcomputer System
Part 3: The Terminal Card

The first two cards of the microcomputer system were introduced in (4) and they themselves constitute a complete CP / M computer in CMOS technology. Only the interface to the user, the terminal, is missing.

Instead of the usual home computer technique of using a portion of the main memory together with suitable logic as a picture store, a separate terminal offers the following advantages:

- The picture and graphic memories can be as large as desired without encroaching upon program memory capability.
- Computer and terminal can be physically separated, the serial connection between them can be quite large (> 100 m) and because of the low data rate, easily protected from electrical disturbances and radiation.
- Eventual processes of a longer nature, such as softscroll, will not block the computer.

The procurement of a terminal offers a few possibilities:

Either purchase it on the flea - market and risk a few nasty surprises such as unsuitable interfaces, missing symbols etc., buy a new low-cost terminal – they cost about 1000 DM – or build the alphanumerical terminal card described here. Only the addition of a keyboard with a parallel output and a monitor are required to make the system operational. Should a keyboard having a serial output be available, it can be connected directly with the computer and drives the terminal card only as a data receiver.

1. DEVELOPMENT AIMS

Anyone who has spent a few hours looking at a bad monitor screen will appreciate the value of a good character representation. Therefore, one of our chief aims was to achieve a good representation of characters. We have only implemented the most necessary facilities, as regards terminal function, as many "bells and whistles" from the user software have not been utilized.

The representation of a character as a 7 x 12 matrix in a 9 x 14 dot field was decided upon as opposed to many terminals which have letters with only 5 x 7 dots. This high character resolution requires that with the usual representation of 24 lines, each of 80 characters, an 18 kHz line frequency monitor would have to be used. It has

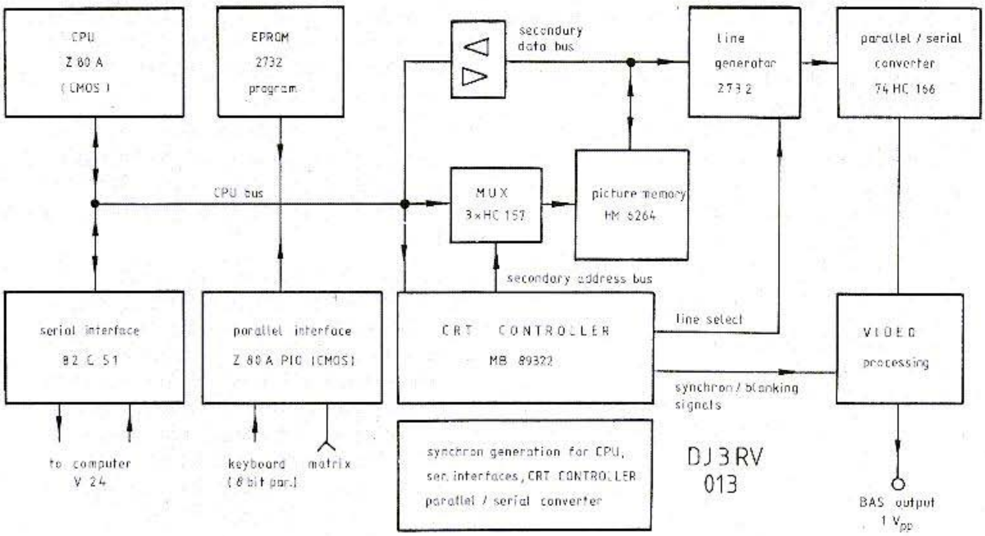

Fig. 1: Circuit diagram of the terminal card

been seen that most TV standard monitors will handle the higher line frequency following an adjustment of the horizontal frequency. The condition is, of course, that the monitor's video amplifier has a bandwidth of at least 20 MHz otherwise all the characters will appear blurred.

If an existing television is required to be utilized, the terminal can switch over to a television standard format with 16 x 64 or 16 x 40 characters. A good monitor with a BAS input and 20 - 25 MHz video bandwidth is, in any case, the best solution. Those who work long hours in front of a monitor screen should have a slightly persistent screen (phosphorous type P 39, GR screen). The reproduction with such a screen, is flicker - free but a quickly changing screen content can cause short - duration ghost images and trails.

When reading long text, the operation of scrolling (i. e. causing the lines to disappear at the top and appear at the bottom of the screen) can become very trying. We have therefore used a technique called "soft scrolling". This makes the picture text, line by line, in a period of 300 ms (selectable) shift automatically upwards thus making reading the text considerably easier.

In order to facilitate the compatibility of proprietary software such as, for example, text processor programs, the majority of the commands have been formulated in such a way that they may be accessed by popular terminals e. g. Televideo 920 / 950. Special functions in a text processor program, such as the deletion and insertion of a line, are also available.

A receiver buffer has been intentionally omitted.

This facility serves to enable slow terminals to have a high baud rate transmission possibility without having a handshake line. This technique, without using additional design sophistication, can result in a serious disadvantage on the monitor screen. If the computer output is inhibited by depressing the ^S key, the transmission stops and the terminal empties the content of the receive buffer, which can contain a few hundred characters and the most interesting portion of the text disappears into the top of the screen.

1.1. Short Form Data Summary of the Terminal Card

- Computer interfaces serial at 9600 baud with handshake lines
- Keyboard connections 8 bit parallel with strobing pulse
- System synchronization 16 MHz either controlled by internal oscillator or optional central synchronizer
- Picture reproduction 24 x 80, 16 x 64 and 16 x 40 lines, softscroll
- Video output BAS signal 1 V_{PP}
- ASCII and German character set
- Construction in CMOS technology, options are also Standard NMOS and LSTTL components

2. CIRCUIT DESCRIPTION

As shown in the diagram of **fig. 1** the terminal card employs a CMOS Z 80 A as the central module. As only a serial line pair is necessary for the computer, an 82 C 51 was used as a serial interface. This contains only a serial interface (as opposed to the Z 80 SIO of the CPU card) but needs only a 28 pin housing.

The keyboard is connected via a Z 80 PIO (CMOS). The second 8 bit port of the PIO upon being switched on, interrogates a matrix which allows a programming of various terminal data (such as transmission format).

The complete sequence control of the screen display is included in the MB 89322. This module represents a development to, and an almost pin-compatible CMOS version of, the Motorola video controller chip MC 6845. In the normal case, the MB 89322 supplies, at its address output, the address for the HM 6264 picture store. The ASCII characters which are stored there are then passed on to the character generator, an EPROM 2732, and converted into a serial dot procession in a shiftregister. Following the addition of the sync. and blanking signals, the completed BAS video signal is ready for use. An additional logic serves to invert either individual characters or the complete monitor screen or to switch over to another degree of brilliance.

With the appropriate keyboard signal, the strobe triggers a processor interrupt via the PIO which causes the immediate transmission of characters to the computer. The receive function then runs normally.

If it is required to write a received character into the monitor memory, the address and data bus of the picture memory is connected to the computer and the video signal meanwhile, is being blanked off. Only the top 4 K from the video controller will be read into the picture memory and displayed on the monitor screen. A proportion of the lower 4 K is used by the processor as a working memory, the rest being free for expansion. The working program is stored in an EPROM 2732.

3. EXPANSION POSSIBILITIES

As there is 8 K EPROM available on the card and also sufficient free RAM, a complete RTTY program or eventually also a packet radio decoder may be incorporated. The card would then be suitable as an autonomous unit for the purposes of digital transmission. Who of our readers will undertake the development of suitable software?

In conclusion a few lines about the graphic display of computer results:

Following the subsequent availability of static CMOS 32 kByte memories, we have decided that the former concept of extending the alphanumeric terminal card should be abandoned and are now designing a colour graphic card with a resolution of 768 x 340 dots, using CMOS, of course. Instead of a colour display, requiring as it does, a very good colour monitor, the three outputs can be combined to deliver a composite signal having eight grey levels – sufficient for simple display representations.

As this project, in spite of the already completed ground work, represents a huge amount of effort, we would request a little patience!

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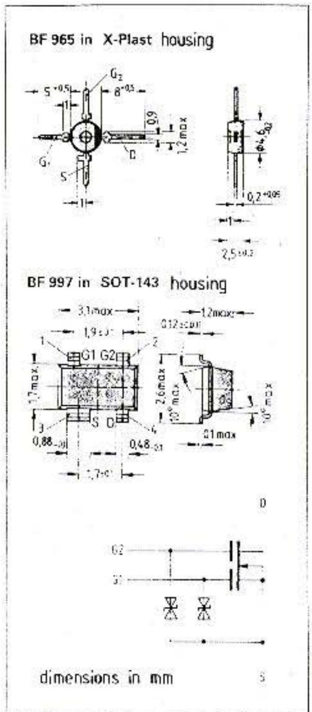
BRIEFLY SPEAKING...

New dual-gate MOS-FET tetrodes BF 965 and BF 997 with suppressed parasitic oscillation tendencies

Parasitic oscillations frequently occur in VHF preamplifiers, which lie much higher than the signal frequency. These undesired oscillations occur owing to parasitic tuned circuits setup in the constructional geometry of the circuit in the environment of the transistor. Assuming that the Q of these tuned circuits is sufficiently high then the parasitics are evident in the range 1 to 2 GHz. The usual practice is to damp these parasitic tuned circuits by means of ferrite beads slipped over G 2 or drain leads of the MOS tetrode. This practice causes extra cost for the beads as well as a somewhat increased space requirement.

Siemens has now integrated a network into the MOS tetrodes BF 964 S / BF 994 S which has no effect in the working frequency range to 500 MHz but above 1 GHz it damps the gain and thereby discourages undesirable oscillations.

The newly developed **BF 965** in an X-plast housing is interchangeable with the BF 964 S requiring no circuit alterations. The electrical specifications and characteristics of a preamplifier so modified do not change with respect to those with the BF 964 S.


BF 965 in X-Plast housing

BF 997 in SOT-143 housing

dimensions in mm

SMD Tuner

This latest innovation is particularly important with regard to the SMD tuner now being developed and housed with the components in the SOT-143 packaging. In this type of housing, ferrite beads are not used. An extensive external parasitic suppressor must be provided which has some influence on the circuit characteristics of the amplifier. These design efforts, together with the extra cost of the suppression components, may be avoided by the employment of the MOS tetrode **BF 997** in the SOT-143 packaging. This has all the same characteristics possessed by the BF 965 but with full suppression properties. It is naturally, fully interchangeable with the BF 994 S.

Short data of BF 965 / BF 997

drain source voltage
$V_{DS} \leq 20$ V

drain current
$I_D \leq 30$ mA

dissipation ($T_U = +60$ °C)
$P_{tot} \leq 200$ mW

rise time
($V_{DS} = 15$ V, $I_D = 10$ mA,
$V_{G2S} = 4$ V, f = 1 kHz)
$g_t = 18$ mS

Power gain ($V_{DS} = 15$ V,
$I_D = 10$ mA, f = 200 MHz
$G_{PS} = 25$ dB
$G_G = 2$ mS, $G_z = 0.5$ mS)

noise figure
(same conditions as above)
F = 1 dB

Siemens Components 23 (1985) ed. 2

Satellite tuner UT-06B (Sanshin)

Tuning range approx. 900-1500 MHz
This unit was mentioned in the article **"SDA 3202 – New PLL IC up to 1.5 GHz"** by Guenter Sattler, DJ 4 LB, in VHF Communications 1/86, P. 18 - 22

Because of the many enquiries, the publishers have decided to make the tuner UT-06B available. **It can be supplied as long as stock lasts.**
Order No.: 6006
Price: DM 175.00

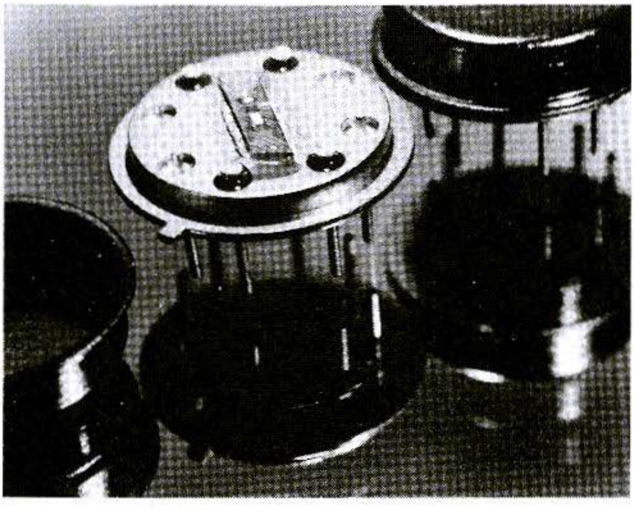
For TV-Sat: Three new surface wave filters

The German Federal Post Office (DBP) has now declared a standard of 479.5 MHz for the second IF of satellite antenna-head receiving down-converters. Previously the choice lay between either 70, 134 and 612 MHz. The new frequency has been the subject of a new Siemens surface wave filter in a DIP 10 housing (Y 6950) and two further filters in metal T0 8 housings (B 527 / 526)

The centre frequency of the newly introduced filters lies uniformly about 479.5 MHz. At the 3 dB points the bandwidth of the filter is 27 MHz (DIP 10 / Y 6950 and T0 8 / B 527), the second metal type (B 526) has a 3 dB bandwidth of 36 MHz. The group delay is 12 ns (DIP 10) and 8 ns (T0 8) peak-to-peak. The typical insertion loss is from 17.5 to 24.4 dB. The amplitude response is given as 0.20 / 0.15 and 0.40 dB.

The plastic type Y 6950 is intended for indoor equipment whereas the metal T0 8 - housed filters (B 527 / 526) are suitable for use in open-air environments in the immediate vicinity of the antenna.

Siemens Press-Info



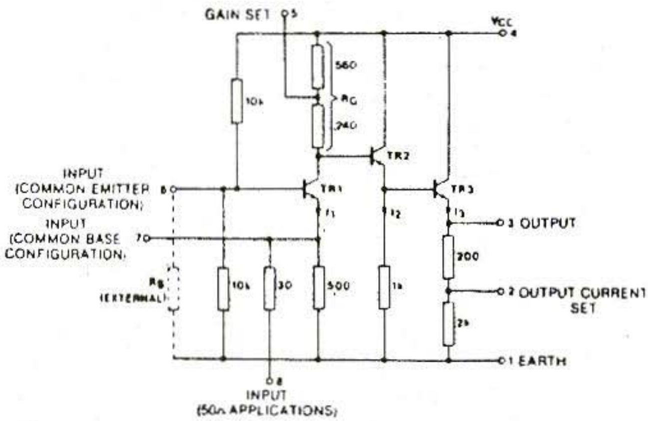


Fig. 1 SL560 circuit diagram

Universal low - noise, wide band amplifier SL 560

This 8 pole IC enables various amplifiers to be constructed whose uses range from low-noise input stages to power output stages, video buffers and on to oscillator circuits. The gain of the amplifier is controllable by means of an external PIN diode. The internal circuit diagram of the IC SL 560 is reproduced in fig. 1. The entire gain of the device is produced in TR 1 which guarantees a well defined, low output impedance. The emitter followers TR 2 and TR 3 decouple the collector from TR 1 and are also responsible for the low output impedance.

Typical data of the SL 560 is:

- amplification: to 40 dB
- noise figure: less than 2 dB
- bandwidth: 300 MHz
- supply voltage: 2 - 15 V

DG 3 CAN

Further information obtainable from Plessey Ltd.

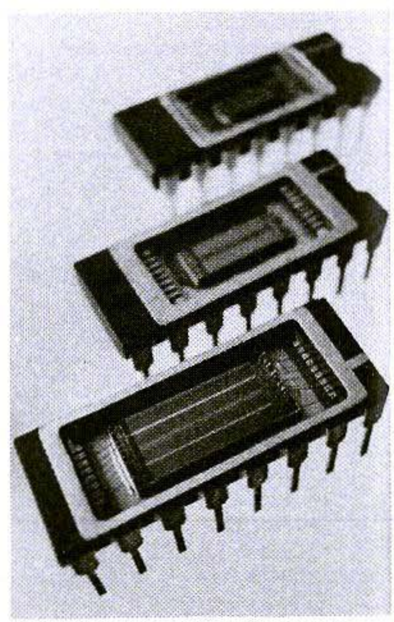
From 1 k to 256 k Dynamic RAMs

The first semiconductor stores for 1024 (1 k) bits, able to both receive information and to give information (read / write), appeared on the market 10 years ago. They were dubbed "random access memories" RAM for short. Siemens concentrated, from the beginning, on the dynamic storage elements, whose information stored as capacitive charges, had to be periodically regenerated but they offered the capability of a high-density integration in the series of MOS chips.

Following the 4 k store came the 16 k (16 384 bit) chip as a spectacular achievement and with it, for the first time, the capability of writing the contents of a complete A 4 page into a single silicon chip. The number of transistors per square millimeter climbed from 400 (1 k) over 500 (4 k) to over 1500 (16 k). There were 36 000 components altogether on a 13.7 mm^2 area. The next times-four leap brought the 64 k store with 180 000 components or 80 000 transistors on a chip area of only 22 mm^2.

Since then, the dynamic world market has specified the 256 k RAM. The HYB 41256 / 57 is for Page- and Nibble-mode function and possesses 320 000 transistors and 260 000 other components integrated on one chip. The 256 k RAM can store the contents of 16 sides of typewriter pages.

Siemens Press-Info



KDI HF Resistors

KDI, famous for a wide range of passive HF components have interesting variants of resistors and resistive networks.

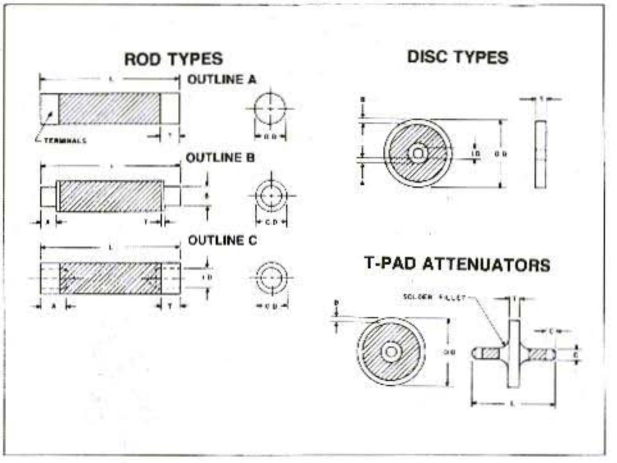
Cylindrical resistors from 10 to 500 ohms at powers of 0.1 Watt to 50 Watt are offered. These resistors are free of inductance and are particularly suitable for terminations (dummy loads) etc.

There are also disc-formed resistors in the range 1 – 225 ohms and powers 2 – 6 Watts with connecting points at the middle and at the edges, which are suitable for very short terminations.

KDI introduce a network which is composed of the above types of component in the form of 50 ohm T-pads. They have attenuations of 1 – 40 ohms and powers of 2 – 7 Watts. They are eminently suitable for incorporation into coaxial plugs. In this application the ring connection of the disc-resistor contacts ground (outer) and the free end of the cylindrical element is connected to the middle plug contact.

All the described resistors cover the frequency range from DC to 18 GHz with a 1 % tolerance.

MICROSCAN, Ismaning,
W - Germany

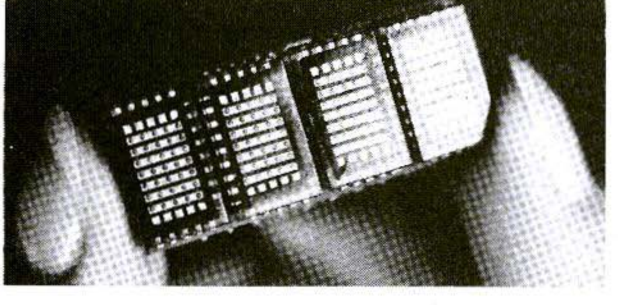


4-Digit Intelligent Matrix Display PD 3435

Besides its LED matrix displays complete with control logic, Siemens now presents this display which allows the brightness, MUX rate, display test and blanking all to be programmed. The new production series PD 3435 is also organized following the 5 x 7 format, the character height being 7 mm. The new matrix display is for the 96 counts and characters of the ASCII code.

As opposed to the previously offered matrix displays, the PD 3435 has four digits and up to seven such displays which may be connected in a row without additional circuitry. The colours available are: orange (PD 3435) and green (PD 3437). An early application for this dot matrix was for travel-ticket vendor machines.

Siemens Press Photo



MATERIAL PRICE LIST OF EQUIPMENT

described in edition 4 / 1986 of VHF COMMUNICATIONS

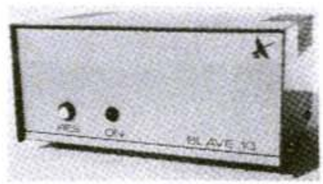
YU3UMV	**TV Satellite Receive System, Part 1**		**Art.Nr.**	**Ed. 4/1986**
YU3UMV 017	**Pre-amplifier**			
PCB	YU3UMV 017	RT / duroid, drilled, silvered	6973	DM 36.–
Components	YU3UMV 017	2 GaAsFET, 1 Z diode, 4 disc caps., 2 feedthru. caps, 4 caps., 7 0204 resistors, 1 each SMA plug and socket	6974	DM 211.–
Kit	**YU3UMV 017 complete**		**6975**	**DM 247.–**
YU3UMV 018	**Converter**			
PCB	YU3UMV 018	RT / duroid, drilled, silvered	6976	DM 46.–
Components	YU3UMV 018	2 GaAsFET, 1 transistor, 1 Z diode 4 disc caps., 4 caps., 2 feedthru. caps., wire, 7 resistors 0204, BNC socket, 1 SMA cable connector	6977	DM 127.–
Kit	**YU3UMV 018 complete**		**6978**	**DM 173.–**
YU3UMV 019	**IF Amplifier (without PCB)**	3 transistors, 1 regulator IC, 5 caps. 4 feedthru. caps., 2 tantalums, wire 6 resistors, 2 BNC panel sockets, semirigid cable		
Kit	**YU3UMV 019 complete**		**6979**	**DM 54.–**
Kits	**YU3UMV 017 to 019** (outdoor unit)		**6981**	**DM 465.–**
DJ3RV/DB1NV	**Microcomputer System, Part 2. The CPU and Floppy Disc Controller**			**Ed. 3/1986**
PCB	DJ3RV 011	Microcomp. CPU	6982	DM 85.–
PCB	DJ3RV 012	Floppy Disc Controller	6983	DM 85.–
32 k EPROM		with monitor program	6984	DM 39.–

New · New · New · Now available ex stock

Interface „slave 10"

for the satellite rotator systems
KR 5400 and KR 5600

Stock-Nr. 1001 DM 590.—
(incl. connection cable)



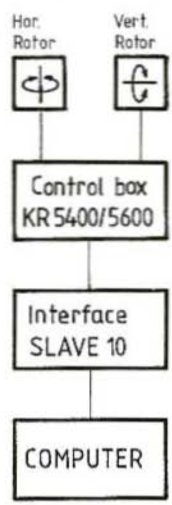
- **fully-automatic antenna tracking system for satellite communications**
- **connection to any computer possible via RS 232**
- **resolution of the dual-channel A / D converter amounts to 10 bits**
- **OSCAR 10 software for the C 64 available**
- **connection to existing rotator systems possible**

Table of commands:

command		response		function
R	CR	R	CR	rotation clockwise
L	CR	L	CR	rotation counter clockwise
U	CR	U	CR	rotation up
D	CR	D	CR	rotation down
S	CR	S	CR	all rotators stop
V	CR	V	CR	rotator stop vert.
H	CR	H	CR	rotator stop horiz.
G xxxxyyyy	CR	G	CR	preset position
F	CR	F xxxxyyyy	CR	interrogation position

xxxx: Vertical position (4 digits)
yyyy: Horizontal position (4 digits)
CR: CARRIAGE RETURN

System's block diagram



Technical data:

Data exchange:	3-wire asynchron. full duplex input and output negative or positive
Data format:	1 start bit 8 data bits 2 stop bits
Baud rate:	1200 B / s
Power supply:	14 V unstab. via control box KR 5400 or KR 5600
Dimensions:	w x h x d = 160 x 80 x 130 mm

Special accessories:

Software on diskette for C 64	Art. nr. 1100	DM 48.—

Satellite rotator systems:

KR 5400	Art. nr. 1013	DM 809.—
KR 5600	Art. nr. 1014	DM 1070.—